TOWARDS HIGH PERFORMANCE GRAPHENE NANOELECTRONICS: MATERIALS, CONTACTS AND INTERFACES

BY

ENRIQUE ALONSO CARRION

DISSERTATION

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Doctoral Committee:

Adjunct Associate Professor Eric Pop, Chair
Associate Professor Xiuling Li
Professor Joseph W. Lyding
Professor Naresh Shanbhag

ABSTRACT

The growth and widespread use of consumer electronics over the last decade has been driven by the evolution and diversification of nanotechnology. In order to continue this growth and implement newer functionalities, such as energy efficiency, speed, flexibility and portability, the scientific community has started investigating an emerging class of materials: two-dimensional nanomaterials.

More specifically, graphene has been at the forefront of this development for a wide range of macro and nanoelectronic applications due to a combination of unique electrical and thermal properties and an atomically thin lattice (~3.4 Å). Some of these applications include flexible transparent electrodes, heat spreaders and fast analog devices and integrated circuits. These large-scale implementations require the ability to inexpensively fabricate wafer-scale pristine graphene sheets with optimized, reliable, and reproducible electrical characteristics. However, challenges such as unstable graphene interfaces, low material quality, high contact resistance and large variability limit graphene performance below theoretical predictions.

In this dissertation work, we investigate these challenges from metrology and technology development perspectives. First we study the graphene-dielectric insulator interface by using a nanosecond-range pulsed characterization technique. Due to gate dielectric imperfections, the drain current degrades, suggesting the presence of charge trapping mechanisms. These charge trapping effects produce threshold voltage instability (hysteresis) in the current-voltage characteristics. We find that with nanosecond-range pulsed operation, hysteresis can be suppressed and reliable intrinsic behavior restored. Additionally, we briefly study the charge trapping contributions of high-field effects.

Next, after having examined intrinsic device operation, we shift focus in order to improve extrinsic device performance. We investigate large-scale CVD-grown polymer-transferred graphene quality issues and characterize device-to-device variability. We optimize a polycarbonate based polymer scaffold, used for mechanical support and protection during graphene transfer, and a vacuum annealing process in order to remove surface residues without inducing damage. Both of these implementations help improve important device parameters such as contact resistance, mobility, and device-to-device variability.

Lastly, we study the interactions at the metal-graphene interface in the presence of increased *p*-type doping. We use known *p*-type dopants in solution (hydrochloric and nitric acid) to induce Fermi level shifts in the graphene-under-metal via surface charge transfer. With this technique, we decrease sheet resistance, increase hole carrier concentration and enhance the metal-graphene electronic coupling. Ultimately these factors contribute to a reduction of contact resistance and its variability, resulting in more reliable and less varying electrical characteristics.

Overall, in this dissertation we have shown experimental work towards the development of higher performing graphene based nanoelectronics. This work contributes to the existing knowledge and techniques and brings graphene nanoelectronic development a step closer to industrial commercialization.

To my parents, Lidia and Enrique, for all the sacrifices they made

to provide us a better life.

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CHAPTER 1: INTRODUCTION

1.1 Evolving and Diversifying Nano and Macro Electronics

Over the past few decades there has been a significant growth in global consumer electronics [1] and in the semiconductor industry [2]. This growth has been the outcome of several socio-economic [3] and technological factors [4]. The development of low-cost powerful nanoelectronics, complex architectures, elaborate algorithms and information processing methods has led to the diversification and extensive use of electronics [4-6]. This technological expansion in consumer electronics is partially reflected in the evolution and widespread use of desktop/laptop computers and mobile devices [7, 8]. Currently, worldwide leading technological companies such as Intel, Samsung, TSMC and Qualcomm compete for larger parts of the consumer market-share [9]. This constant competition has resulted in the development of new innovative products leading to the diversification of nano- and macro-electronics.

This diversification has been driven by following Moore's law, an observation and prediction about the number of transistors in computer processors [10]. Its success is exemplified by examining the constant increase in number of transistors and operating frequencies in CPUs since the early 1970s as shown in Figure 1.1(a-b). However, keeping up with this prediction has become more challenging as technology nodes have advanced into the nanometer scale [11, 12]. In particular, detrimental short-channel effects such as drain-induced barrier lowering (DIBL), higher sub-threshold currents (off-state leakage) and channel length modulation result in lower drive current levels, higher off-state leakage (and static power dissipation [13]) and threshold voltage instabilities [14]. In order to overcome

these issues and to maintain Si CMOS device scaling, new device structures have been implemented or proposed, such as silicon-on-insulator (SOI), double-gate, tri-gate devices and gate-all-around devices [Figure 1.1(c-d)]. Nevertheless, to continue advancing the development of nano- and macro-electronics it is necessary to further improve existing functionalities (such as speed and energy efficiency) and implement new capabilities (such as portability and flexibility). With this framework in mind, the scientific community has been exploring alternative materials for the past several decades and more recently two-dimensional (2D) materials have attracted increased attention.

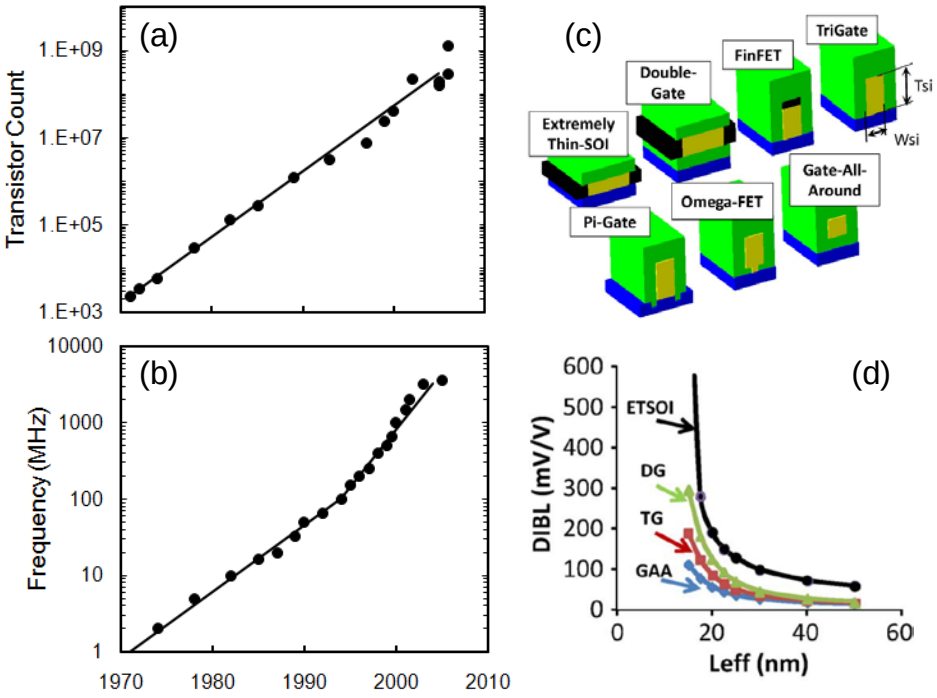

Figure 1.1. (a) Number of transistors (b) and operating frequency of Intel CPUs since 1970 until early 2000s, when traditional MOSFET scaling was used. Reproduced from Ref. [15] © [2011] IEEE. (c) Different device geometries/architectures developed and proposed in order to mitigate detrimental short-channel effects. (d) Drain-induced barrier lowering (DIBL) as a function of effective channel length (Leff) for the device architectures presented in panel (c). Panels (c) and (d) reproduced from Ref. [14] © [2012] IEEE.

Two-dimensional materials consist of atomically thin layers held together by van der Waals forces. They exhibit unique mechanical, thermal and electronic properties [16, 17] which potentially could serve to enhance functionality of current CMOS technologies [18] and access new capabilities in regimes/environments which traditional rigid semiconductors cannot access [19-21]. For example, their intrinsic optical transparency (in the visible range) and flexibility make them promising candidates for transparent conductors [22] or applications in flexible electronics [23, 24]. Furthermore, by taking advantage of their metallic (graphene), semiconducting (transitional metal dichalcogenides) or insulating nature (hexagonal boron nitride), more complex heterostructures with diverse functionalities can be implemented [19, 21]. Ultimately, the innovation of electronics will be driven by our ability to expand new functionalities, while new materials will prove to be an important vehicle for this development.

1.2 Graphene Historical Background and Basic Physical Properties

Graphene has been one of the most promising and studied two-dimensional nanomaterials over the past decade due to a combination of unique electrical [21, 25, 26] and thermal [16, 27] properties and an atomically thin lattice (~3.4 Å). The first sheet of monolayer graphene was obtained in 1962 [28] by the reduction of graphite oxide; the name “graphene” itself was coined in 1994 [28]. In 2004, a single monolayer of this 2D material was isolated by mechanical exfoliation and modulation of carriers was demonstrated [29]. Since then, interest in graphene related research has surpassed expectations. Furthermore, promising advances in the synthesis [30-32], characterization of electrical and thermal

physical properties [16, 21, 25-27] and implementations as transparent electrodes [33-35], heat spreaders [16, 27, 36] and fast analog devices and integrated circuits [37-39] have been reported. However, these works have also highlighted several technical challenges and intrinsic limitations in the potential of this material [40-42] (such as the lack of a band-gap, its chemically inert nature, presence of structural defects and high contact resistance).

Currently, the scientific community channels research efforts towards advancing graphene large scale manufacturing and processing aimed towards developing Si CMOS back-end components (such as interconnects, isolation layers, heat spreaders, etc.) or other more specialized applications (such as flexible displays, transparent electrodes, biosensor, batteries among others). With this historical background and broad perspective in mind, we start looking at the basic physical phenomena which have made graphene such an exciting and promising material.

Graphene is an atomically thin (~3.4 Å) sheet of sp^2 covalently bonded carbon atoms arranged in a honeycomb hexagonal lattice as shown in Figure 1.2(a). Atoms share a π-bond with their three nearest neighbors resulting in the formation of valence and conduction bands. The resulting band structure [Figure 1.2(b)] is symmetric and linear near the *K* and *K′* symmetry points, resulting in high and equal intrinsic electron and hole room temperature mobility (10,000 $cm^2V^{-1}s^{-1}$ or higher at room temperature). In contrast, transistor materials from Si and Ge to III-V compounds have reasonably good electron mobility (up to 800 $cm^2V^{-1}s^{-1}$ for Si electron inversion layers and 30,000 $cm^2V^{-1}s^{-1}$ for InAs and InSb quantum wells), but hole mobility four to thirty times lower (200 $cm^2V^{-1}s^{-1}$ for Si hole inversion layers and up to 1000 $cm^2V^{-1}s^{-1}$ for strained InSb) [43].

Additionally, graphene's phonon dispersion relation, shown in Figure 1.2(c), yields highly energetic optical phonon branches (~160 meV or 5x greater than Si optical phonons), and as a result a remarkably high thermal conductivity (~3000 – 5000 $W \cdot m^{-2}$) has been theoretically calculated and measured [44]. Finally, the high natural abundance of carbon (compared with some of these other rare earth metals like In or Sb [45]), high optical transparency and mechanical flexibility (due to atomically thin lattice) are other encouraging motivations to develop graphene for a wide range of existing and new applications (such as developing nanoelectronic components and devices which operate in environments where traditional crystalline rigid semiconductors may not easily access).

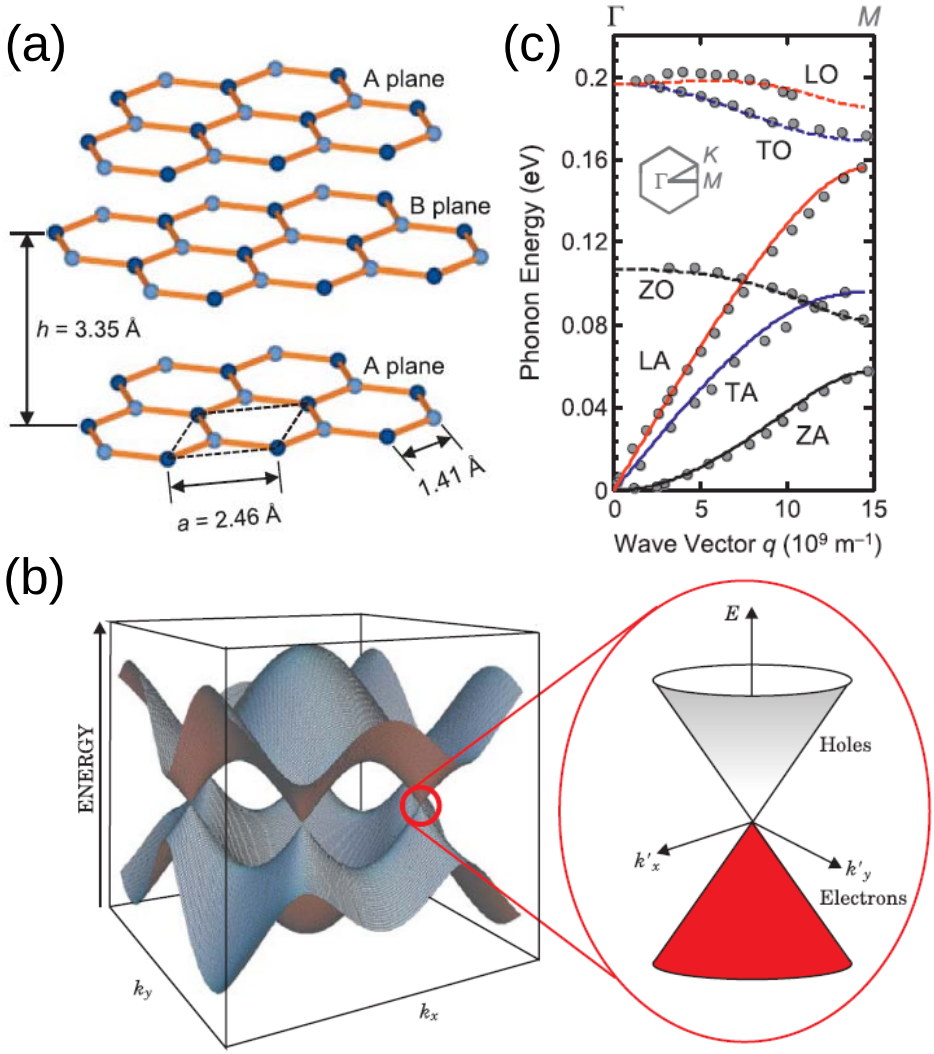

Figure 1.2. (a) Schematic of graphene hexagonal lattice showing graphene interlayer spacing of h = 3.35 Å. Bottom sheet shows unit cell (dashed lines) with lattice constant of a = 2.46 Å. (b) Graphene electronic band structure. Inset shows energy dispersion relation around K and K' symmetry points showing the Dirac cone (region where conduction and valence band intersect). (c) Phonon energy spectra from the Γ-to-M crystallographic direction. Note longitudinal and transverse optical phonons have energies of ~0.16 eV near the M symmetry point. Panels (a) and (c) reproduced from Ref. [16], with permission from Cambridge University Press and panel (b) reproduced from Ref. [17] with permission from the American Physical Society.

1.3 Other Two-Dimensional Nanomaterials

More recently, over the past 3 to 4 years, two-dimensional materials other than graphene have also attracted great interest. A whole new family of materials called transitional-metal-dichalcogenides (TMDCs) present promising structural, mechanical, optical and electronic properties [20, 46] similar to those of graphene, but with the additional benefit of a band gap. The first one of these materials to gain attention was molybdenum disulfide (MoS_2), shown in Figure 1.3(a). A single monolayer of this material was first isolated (via mechanical exfoliation) and electrically characterized by Kis *et al.* in 2011 [47]. Since then, a plethora of other TMDC have been exfoliated (or synthesized [48]) and studied theoretically [49, 50] and experimentally [51-53]. Even more, individual nanoelectronic devices [47, 54] and larger circuit architecture [55, 56] have already been demonstrated. This rapid progress of TMDC based electronics, combined with the benefits from their monolayer nature and electronic band structure, demonstrate great potential.

Lastly, due to the atomically thin nature (one to few atomic layers) of TMDCs, integration with other 2D nanomaterials such as graphene (semi-metal) and hexagonal boron nitride (insulator) [Figure 1.3(b)] is plausible [19, 21]. This interlayer integration has already been demonstrated in field-effect transistors using semiconducting channels of tungsten diselenide (WSe_2) [57] and molydinium disulfide (MoS_2) [24], with hexagonal boron nitride (hBN) gate dielectrics and graphene metallic gate electrodes [Figure 1.3(c)]. Further development of these and other types of architectures, such as tunneling transistors [58, 59] or memory devices [60], would help the advancement of nano- and macro-electronics, and open up new avenues towards closer interactions between electronics, people and their environments.

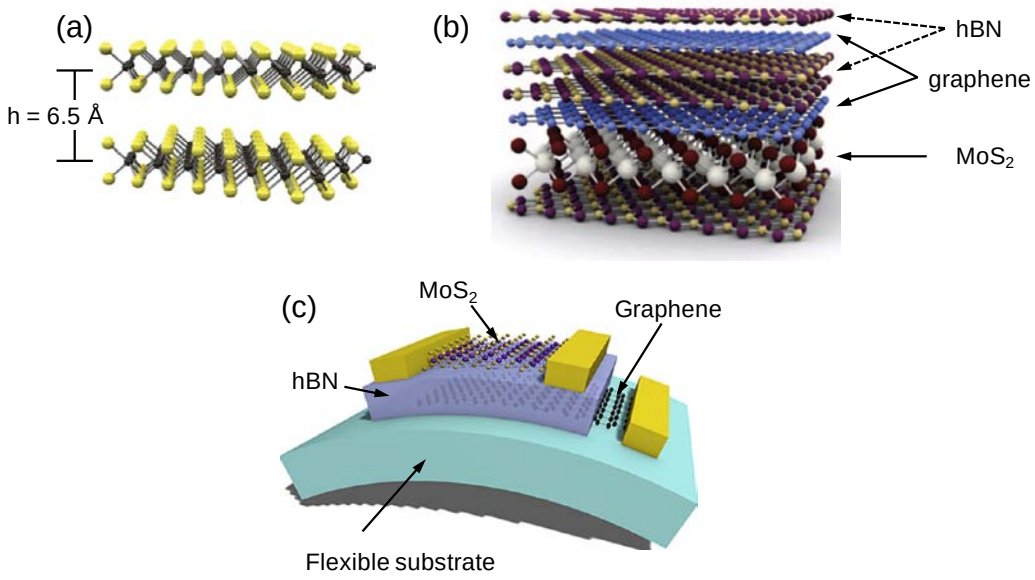

Figure 1.3. Schematic of (a) of molybdenum disulfide (MoS2) showing interlayer spacing of h = 6.5 Å. Adapted by permission from Macmillan Publishers Ltd: Nature Nanotechnology [47]. (b) MoS_2, graphene and hexagonal boron nitride (hBN) heterostructure. Adapted by permission from Macmillan Publishers Ltd: Nature Nanotechnology [21]. (c) MoS_2, graphene and hexagonal boron nitride (hBN) flexible transitor. Reprinted (adapted) with permission from [24] respectively. Copyright (2013) American Chemical Society.

1.4 Organization of Dissertation

In this study, we investigate different aspects for the improvement of two-dimensional graphene based nanoelectronics. In the previous sections, we presented the framework of evolving nano- and macro-electronics, introduced graphene and its most relevant physical properties and described how it can help to fill new voids as technology evolves. Finally, we briefly described other two-dimensional nanomaterials that can also serve to complement graphene and CMOS technologies.

In Chapter 2, we review the fundamentals of graphene nanoelectronics. We first define and differentiate intrinsic-like and extrinsic electrical properties. Next we present a thorough review of the current graphene challenges and classify them into interface, quality and contact issues. We highlight the main approaches the research community has taken to

address each one of these hurdles and describe how our work contributes to ongoing developments.

In Chapter 3, we present the first one of these contributions by studying the graphene-high-κ dielectric interface by using nanosecond pulses. With this measurement technique, we characterize charge interface and bulk trapping time constants, and we manage to circumvent some of the detrimental factors which negatively affect transport and recover hysteresis-free electrical characteristics. Additionally, we present high field measurements and their role in charge trapping and hysteresis.

In Chapter 4, we investigate the electrical quality and variability of polymer transferred graphene field effect transistors. Depending on which polymer layer and corresponding anneal conditions are used we find that contact resistance and mobility variability are a result of non-homogeneous doping levels and spatially variable strain.

In Chapter 5, we study graphene doping via surface charge transfer and its effects in Raman and UV-photo spectroscopy measurements. Additionally, we study the electrical characteristics of *p*-type doped graphene channels and contacts before and after the same vacuum annealing process optimized in Chapter 4. This study finds that surface charge transfer is a viable way of tuning the electrical properties of graphene and leads to reduction of electrical variability.

Finally, in Chapter 6, we present the conclusions for our work, highlight the areas in which our work contributes to the development of graphene nanoelectronics and describe important future research directions.

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CHAPTER 2: GRAPHENE FIELD-EFFECT TRANSISTOR FUNDAMENTALS

Owing to a combination of unique electrical [1] and thermal [2] properties mentioned in detail in Chapter 1, and due to its atomically thin lattice (~3.4 Å), graphene has become a promising material for applications including flexible transparent electrodes [3-5], heat spreaders [2, 6] and fast analog devices and integrated circuits [7-9]. All these applications use graphene in different configurations and structures; however they heavily rely on the electrical characteristics of the material. For this purpose, in this chapter we review graphene's basic electrical properties, define differences between intrinsic and extrinsic electrical characteristics, discuss the main challenges ahead and address the advantage of employing a field-effect structure as a developmental platform.

2.1 Intrinsic and Extrinsic Electrical Characteristics

As we mentioned in the previous chapter, graphene is a promising material for nanoelectronics due to unique electronic properties such as a high intrinsic mobility [10]. In this section we define intrinsic and extrinsic electrical characteristics and highlight their main differences. For example, several works [11-13] strictly define intrinsic graphene properties as those that are measured in fully idealized conditions in which no free carriers are present (T = 0 K and with the Fermi level exactly at the charge neutrality or Dirac point). However, by this definition any experimental and realistic graphene system measured at $T \neq 0$ K or even with a Fermi level slightly above or below the point of charge neutrality (where the

conduction and valence band meet) will have free carriers available and be considered extrinsic. This definition is of theoretical importance in order to study the fundamental physics of the material; however, it is not convenient in order to distinguish electrical characteristics affected by experimental extrinsic effects.

In this work, we define intrinsic and extrinsic graphene electrical properties by considering the conditions that can be experimentally achieved. We refer to intrinsic-like graphene properties, those measured in conditions under which the main detrimental factors affecting transport can be significantly minimized or avoided; these factors include detrimental substrate interactions (i.e. doping, remote phonon scattering, etc.) [14, 15], high impurity levels ($>10^{11}$) [16], high contact resistance values [17] and grain boundary effects [18, 19]. On the other hand, extrinsic graphene properties will exhibit slightly degraded characteristics because of these detrimental effects.

Figure 2.1(a) highlights intrinsic-like electrical characteristics (red solid line) from Ref. [20], which experimentally minimizes a number of these effects. Here, suspended pristine exfoliated graphene is used in order to remove graphene-substrate interactions and grain boundary effects. Also, the measurements are done at cryogenic temperatures ($T \approx 5$ K) to minimize impurities scattering and reduce thermally generated carriers. Finally, graphene undergoes a current annealing process to remove surface impurities while its electrical characteristics are measured using a Hall technique to avoid detrimental contact resistance. As a result of the combination of these factors, we observe (red solid line) a symmetric gate-controlled resistivity (ρ) with sharp and narrow features when the gate voltage (V_G) approaches the Dirac point (V_0, point of maximum resistivity or minimum conductivity) and a saturated-like smaller resistivity at higher gate voltages ($|V_G| > V_0$). On the other hand,

extrinsic typical characteristics for a substrate supported graphene device (blue dashed line) exhibit a higher and broader resistivity (ρ) when $V_G = V_0$ and $|V_G| > V_0$.

Overall, the electrical characteristics in the intrinsic-like (suspended) and extrinsic (supported) cases exhibit ambipolar transport modulated by the gate (which in turn moves the Fermi level accordingly); however, three major differences [marked in Figure 2.1(a)] can be readily distinguished in the intrinsic-like case: (1) higher minimum conductivity ($\sigma_0 = 1/\rho(V_G = V_0)$), (2) higher mobility and (3) lower contact resistance.

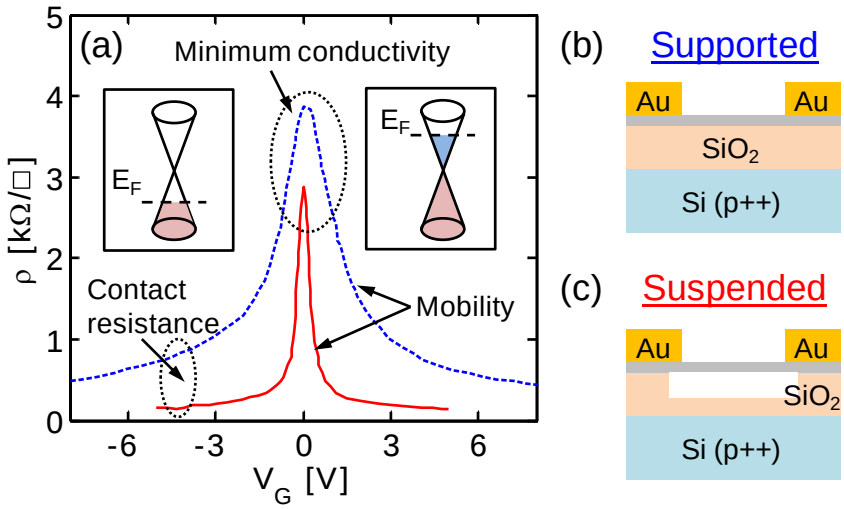

Figure 2.1. Electrical transfer characteristics measured at $T = 5$ K for exfoliated suspended graphene (intrinsic-like) and SiO_2/Si supported graphene (extrinsic) adapted from Ref. [20] with permission from Elsevier. We note that ambipolar transport arises as the graphene Fermi level moves from the valence to the conduction band. Additionally, we labeled how minimum conductivity, mobility and contact resistance differ for the cases.

In the case of minimum conductivity for intrinsic-like samples, the lower presence of charged impurities [11, 12] results in decreased impurity scattering and lower intrinsic carrier concentrations [21], while the opposite situation applies to extrinsic substrate supported samples (blue dashed line). We note that these trends apply in the limit of channel width larger than the length, in which confinement effects do not alter the electrical properties.

Additionally we note that measuring and calculating a universal intrinsic minimum graphene conductivity has been a controversial area of discussion/research over the past several years [11]; contradicting results have been obtained depending on different physical assumptions and models. Ultimately, reaching a "universal" minimum conductivity value is outside of the scope of our research.

In the case of mobility, we examine the slope of the resistivity near V_0 to quickly determine an estimate for field-effect mobility. We observe that the intrinsic-like suspended case (red solid line) has a higher slope (transconductance) and hence also a higher mobility value than that of the extrinsic supported graphene case. Furthermore, a more rigorous calculation [20] finds mobility values as high as 230,000 $cm^2V^{-1}s^{-1}$ for the intrinsic-like suspended case, while in the extrinsic supported graphene case values can range from ~1,000 to 10,000 $cm^2V^{-1}s^{-1}$. This drastic contrast of mobility values is primarily caused by lower amount of charged impurity carriers in the absence of a substrate and after a current annealing process.

Lastly, the saturated-like region of measured resistivity corresponds to higher or lower values of contact resistance. In general, contact resistance is generated as electrons are injected from the metallic carrier reservoir into the conducting graphene channels [22]. More specifically, carriers are injected from the metal contact into the graphene-under-metal and subsequently transported to the graphene gate-controlled channel. We will explore and explain both of these processes in more detail in the section 2.2 and in Chapter 5, but for now it is important to note how higher or lower contact resistance values affect the transfer characteristics.

Next, we examine the output characteristics (drain current, I_D vs. drain voltage V_D) of typical graphene transistors, the physics behind their different operation regimes and compare the differences between intrinsic-like and extrinsic behavior. Figure 2.2 shows typical output characteristics for a graphene field-effect transistor (GFET). We see that as the drain voltage (V_D) is increased [Figure 2.2(b-d)], the carrier density towards the drain side of the channel decreases, the electric field increases and the drain side graphene channel resistivity increases in an analogous manner to conventional pinch-off region formation in Si MOSFETs. Additionally, in the case of graphene (a semi-metal with no band gap) when the V_D created drain side is larger than that at the Dirac point, the type of conductivity reverses from electrons to holes (or vice versa), carrier density increases once more and I_D increases linearly. This ambipolar behavior limits the region over which graphene devices exhibit current saturation depending on channel and device electrostatics [23, 24]. Moreover we note that other factors besides electrostatics alone, such as self-heating [25] and velocity saturation [21, 26], also contribute towards current graphene current saturation.

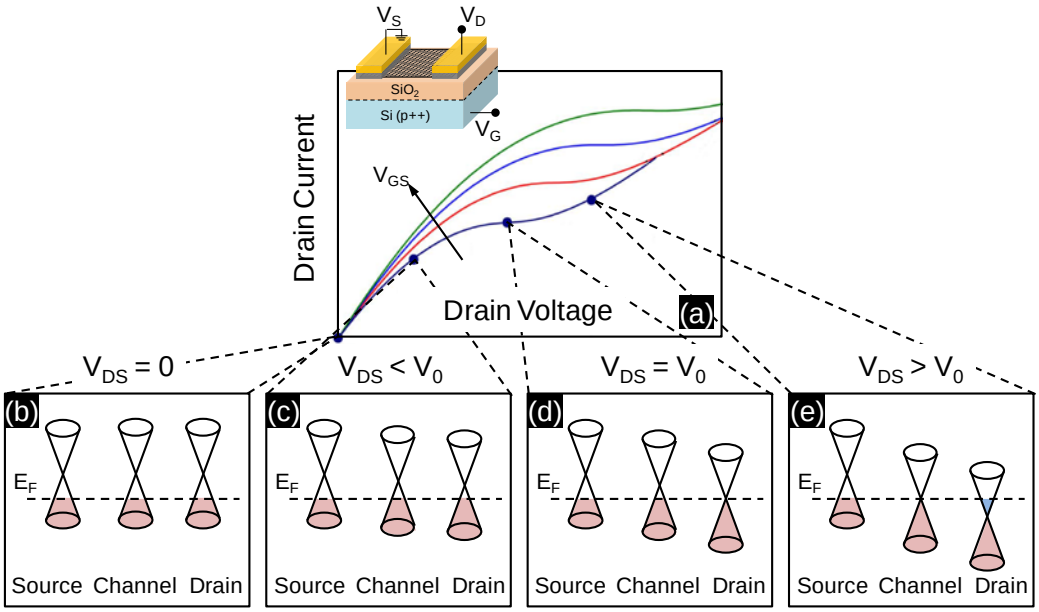

Figure 2.2. (a) Drain current (I_D) as a function of drain voltage (V_D) for many gate-to-source voltage conditions (V_{GS}) for a representative graphene FET (adapted from Ref. [23] © [2013] IEEE). Inset shows device schematic and biased terminals. Four drain-to-source voltage (V_{DS}) points are highlighted (blue dots) in I_D-V_D curve, with representative distribution of carriers along the channel in each case: (b) V_{DS} = 0 V, (c) $V_{DS} < V_0$, (d) $V_{DS} = V_0$ and (e) $V_{DS} > V_0$.

Finally, in a similar manner as observed in the transfer characteristics (Figure 2.1), detrimental effects such as charged impurity trapping and contact resistance also manifest in the output characteristics. In the case of the former, charge impurities from the substrate or the graphene-gate insulator interface (or bulk) can partially screen the gate voltage and drastically reduce electrostatic control [27, 28]. As a result, current saturation can be in extreme cases almost completely suppressed. In the case of the latter, high contact source and drain series resistances (i.e. contact resistance) affect the transport drastically. In particular, as channel dimensions are reduced below ~1 μm, they can dominate transport, as shown in Figure 2.3. Furthermore, when current saturation is degraded or suppressed either due to screening of the gate or high contact resistance, other important device parameters, such as

output conductance (g_d), transconductance (g_m), gain (A_V), cut-off frequency (f_T) and maximum operation frequency (f_{max}) are also heavily degraded.

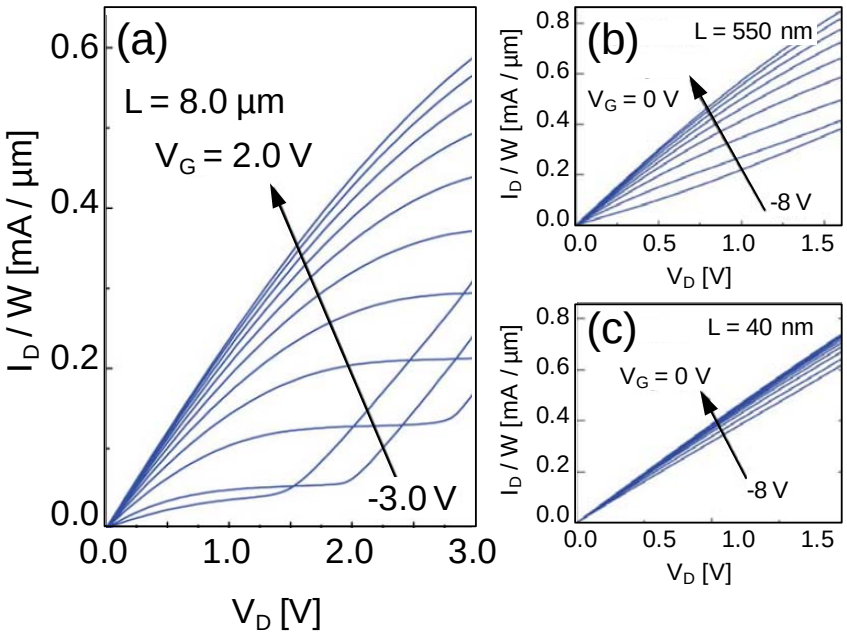

Figure 2.3. Drain current (I_D) normalized by channel width vs. drain voltage (V_D) characteristics for graphene FETs of three different channel lengths: L = 8.0 µm, 550 nm and 40 nm. Adapted from Ref. [27]. © [2013] IEEE.

2.2 Graphene Challenges: Interfaces, Material Quality, and Contacts

As we have seen in the previous section there are many detrimental effects that currently prevent graphene electronics from reaching their intrinsic potential. In this section, we review and explain in more detail the present challenges of graphene based electronics. Additionally, we summarize in each case some of the key approaches currently being pursued, and describe the methodologies that we will follow in Chapters 3, 4 and 5 in order to address these issues. In general, there are three main obstacles in the development of graphene electronics: 1) graphene interfaces, 2) graphene material quality and 3) contact resistance.

A. Graphene Interfaces: For most applications on nanoelectronics, graphene needs to be placed on an insulting substrate and/or covered with other isolating materials. More specifically, in the case of GFETs, the most basic configuration requires an insulating substrate in order to isolate its electrical properties and a dielectric material that serves as a gate insulator. In some cases, the insulating substrate can also be used as a gate dielectric; however, this situation is not optimal for nanoelectronic devices, where localized control of each gate is desired (gating graphene through the substrate would result in a global gate). The main issue with the substrate, the gate dielectric and their interfaces with graphene is that they can store fixed and mobile charges at the interfaces and within the bulk of these insulators [11, 12, 29], resulting in detrimental transport effects.

More specifically, in the case of an amorphous SiO_2/Si substrate (a widely used substrate) fixed charge puddles [29, 30] and mobile charges are known to form at the interface [31, 32] and within the bulk of the dielectric [33-35], resulting in transient and non-homogeneous charge distributions in the channel. These charges affect the stability of electrical properties and generate hysteretic effects in the electrical characteristics [31]. Additionally, charge puddles result in an increase of minimum carrier density which leads to broadening of states near the Dirac point [30, 36] and increases impurity Coulomb scattering [12, 13]. Furthermore, these problems are not unique to the graphene-SiO_2 interface; they also occur between graphene and other amorphous and crystalline insulators [36-39]. Even more, in the case of crystalline high-κ gate insulators grown via atomic layer deposition (ALD), more complex interface interactions arise since an additional a seed layer is necessary [40]. These bulk and interface charges can partially screen the gate and decrease channel electrostatic control [27, 28].

In general, these interface problems have been approached from a process-development and a characterization perspective. In the case of the former, a different number of implementations have been demonstrated, such as chemical treatments [41], anneals [42-45], substrate engineering [46] and high-κ dielectric implementations [37, 40, 47]. In particular, some of the research in substrate engineering has resulted in the development and implementation of another two-dimensional nanomaterial, hexagonal boron nitride (h-BN). This insulator has emerged as one of the best material candidates for graphene integration due to its inert crystalline structure with no dangling bonds, high phonon energies [14], wide band gap and ultraflat surface (see Figure 2.4) [29]. These factors combine to drastically reduce impurity charges and their spatial non-homogeneity at the interface compared to a SiO_2 substrate, as shown in Figure 2.4(c-d).

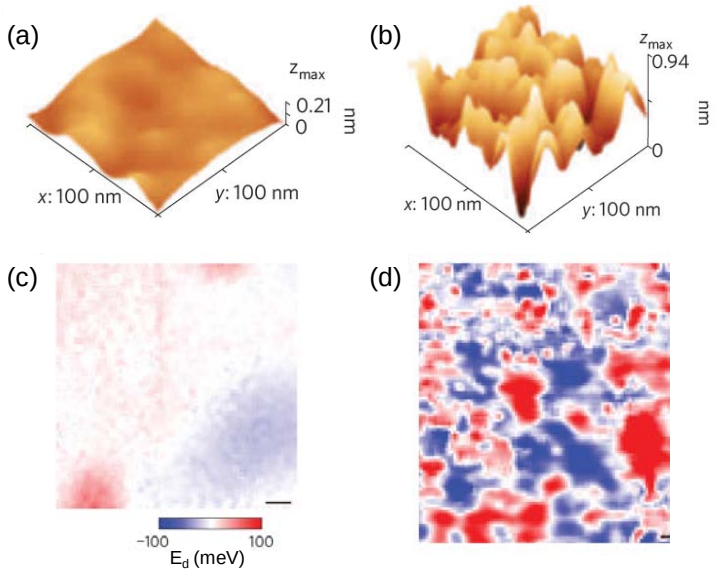

Figure 2.4. (a) STM topographic image of graphene on h-BN and on (b) SiO_2. (c) Spatial maps of the density of states of graphene on h-BN and (d) SiO_2. Blue and red regions indicate the non-homogeneous charge distribution (either electrons or holes) in each sample. Note that charge is distributed more evenly for the graphene on h-BN sample. Adapted by permission from Macmillan Publishers Ltd: Nature Nanotechnology [29].

This reduction of charged impurities leads to enhanced graphene electrical characteristics. For example, recent efforts have demonstrated room temperature graphene motility values ranging from 10,000 to 100,000 $cm^2V^{-1}s^{-1}$ for exfoliated graphene on top of exfoliated [10, 48, 49] and CVD-grown [50] h-BN films. These values are similar to those obtained for suspended exfoliated graphene FETs (Figure 2.1), where substrate detrimental effects are removed. Additionally, other types of device structures, such as tunneling devices, have also been proposed and demonstrated [51, 52]. Current efforts in h-BN and graphene integration are geared towards large-scale growth of h-BN-graphene heterostructures [53, 54].

In the case of the second perspective, the electrical characterization of graphene-interface issues, much work has also been done over the past few years. Some efforts have focused on characterizing the graphene-SiO_2 interface by examining transient current behavior and using different voltage sweep rates [15, 34]. Unfortunately, these measurement techniques are not capable of probing transient trapping events which can occur in the short time scales (micro- to nanoseconds). Furthermore, the graphene-high-κ dielectric interface, important to achieve good electrostatic control of the channel, has not been characterized as extensively as the graphene-SiO_2 interface. One study in particular showed that by using a pulsed measurement technique to measure the output characteristics, trap screening of the gate voltage was reduced and electrostatic gate control enhanced [28]. However, even this work did not characterized the time constants associated with trapping of carriers or examine the trapping in the transfer characteristics. With this framework in mind, we present a nanosecond pulsed measurement technique (Chapter 3) capable of probing bulk and interface

trap defects in nanosecond time scales [31]. We use this technique to extract corresponding trapping time constants and recover repeatable and reliably electrical characteristics.

Finally, we note that despite the advances in the synthesis of h-BN and its integration with graphene, high-κ materials will still be necessary in order to achieve optimum electrostatic control of the channel (h-BN has a dielectric constant similar to SiO_2, ~4.0).

B. Material Quality: All large-area graphene implementations require the ability to fabricate wafer-scale materials with optimized, reliable, and reproducible electrical characteristics. To this end, epitaxial growths and chemical vapor deposition (CVD) have emerged as the leading growth techniques. The former technique is a top-down process which was first developed in the early 1960s [55]. It relies on the thermal reduction on the C-face of SiC substrates resulting in the formation of one or two layers of graphene on the Si surface. However, issues such as monolayer graphene isolation from remaining Si substrate underneath [56], spatial variations in larger area growths, the highly doped nature of graphene obtained [57], the inherent wastefulness of this process (SiC wafers are consumed during this process) and its high cost (SiC wafers are significantly more expensive than Si) undermine the large-scale implementation of this technique.

Contrarily to epitaxial growths, CVD is a bottom-up technique in which precursors molecules are deposited on catalyst substrates in a self-limiting high temperature (usually at ~1000 °C) reaction [58-60]. This reaction can be carefully controlled by adjusting the type and flow of precursor molecules [61, 62], the pressure and temperature [58] and the catalyst substrates employed [63, 64]. Many research groups have demonstrated the ability to grow high quality large-area (in the order of a few centimeters) single-crystal monolayer and multilayer graphene materials on Ni [65], and Cu [58], resulting in electrical characteristics

comparable to those of pristine exfoliated graphene. Even more, the inherent presence of grain boundaries [19, 66], which degrade electrical [67] and thermal [68] transport, has recently been minimized/eliminated by using Ge substrates [69]. Overall, all of these features, such as flexibility, high-quality and low-cost make CVD one of the most promising techniques to employ in the large-scale implementation of high quality graphene films.

However, despite the great potential of CVD processes and the high quality material they yield, graphene obtained in this manner often requires transfer from the initial catalyst substrates to other insulating substrates [70]. This transfer is often performed using a sacrificial polymer scaffold for protection and mechanical support, and as a result the graphene properties exhibit substantial electrical variability [71]. Furthermore, while much effort has been devoted to improving electrical characteristics through substrate engineering [27, 48, 72], high-k dielectric scaling [37, 40] and graphene surface treatments and anneals [42, 71, 73], the physical sources of the electrical variability in polymer transferred graphene and how they might be controlled or minimized remain poorly understood. For these reasons, in Chapter 4 we investigate and quantify the role of electrical variability of graphene based FETs grown by a CVD method and transferred using three different polymer scaffolds.

C. Contact Resistance: Another important area of research which greatly hinders the performance and delays the industrial development of graphene based nanoelectronics is contact resistance. This parasitic effect stems from graphene's chemically inert nature to which covalent bonds cannot easily be formed [74]. Moreover, while its atomically thin lattice may present certain advantages such as potentially mitigating short-channel effects (similarly to SOI or UTBSOI [75]) or ideal electrostatic channel control, it also makes it difficult to interstitially create highly doped or silicide-like contact regions like in

conventional Si CMOS. Furthermore, compared to state-of-the-art Si CMOS which exhibits contact resistance values ~80 Ω·μm (or ~10% of the on-resistance, such that $R_C = 0.1 \times R_{ON} = 0.1 \times V_{DD}/I_{ON}$ [57]), R_C is larger in graphene devices by factors ranging from 2-10x [17, 76, 77].

In general, contact resistance in graphene is caused by physical interactions with the contact metal. More specifically, two sequential processes can be used to describe this interaction: 1) carrier injection from the metal to the graphene underneath 2) followed by transport to the gate-controlled channel. In the case of the former (metal-to-graphene injection), a dipole and a built-in potential form at the metal-graphene interface due to their weak electronic coupling and Fermi level differences [17]. These effects result in current crowding at the contact edges with graphene-to-metal (or vice-verse) carrier injection occurring over a specific distance inside the contact: the transfer length (L_T, distance over which the V_{DS} generated potential drops to 1/e). Additionally, the small density of states available near the Dirac point complicates carrier injection even further. For the latter processes (transport to the gate-controlled channel) an additional built-in potential forms due to the metal induced charge transfer doping of graphene thus modifying E_F. As a result, asymmetric transfer characteristics are observed [76, 78] depending on the electronic nature (*n*- or *p*-type) of the graphene-under-metal with respect to the channel.

In order to improve contact resistance issues, several methodologies have been employed over the past few years. One of the most common techniques relies on Fermi level pinning by tuning the graphene work-function using different metals [77, 79] or substrate chemical treatments. However, the level of these techniques have demonstrated has been limited and inconsistent. Others have tried implementing annealing processes [42, 43],

cleaning techniques [73, 80] and partially induced graphene damage in order to increase the electronic coupling at the metal-graphene interface. And while there has been some encouraging demonstration in which R_C is decreased, the lack of control and reproducibility remain an obstacle. Furthermore, other recent works [57, 81, 82] have shown early promise by implementing side-contact geometries (also called end-contact) which inject carrier from the graphene edges as well as the top thus reducing R_C down to ~100 Ω·μm [57, 82]. However, it was also reported [81] that these implementations can significantly increase the transfer length (L_T) at the metal-graphene interface, resulting in increased overall resistance and lower drive currents as contacts length (L_C) becomes smaller than L_T [76, 83]. With this framework in mind, we present work in Chapter 5 that directly addresses contact resistance issues by attempting to modulate the graphene work-function underneath the metal through surface charge transfer doping. In this way, we demonstrate R_C improvements comparable to those described earlier and severely reduced deice-to-device variability.

2.3 Field-Effect Transistors as a Developmental Platform

Up to this point, we have presented and explained the underlying physical processes of the main areas of research in the advancement of graphene nanoelectronics. Additionally, we surveyed some of the approaches followed by various research groups and briefly described our work within the respective framework. The approaches we presented are geared towards the development of graphene based nanoelectronics (in particular transistors); however, we believe there is another important perspective worth highlighting. Field-effect transistors provide a platform in which all of the main issues described in the Section 2.2 (interfaces, material quality and contacts) can be directly modified and characterized while measuring

their impact on performance. More importantly, these issues are not specific to transistors; many other potential applications of graphene such as flexible displays [84], transparent and flexible electrodes [4, 5, 85], interconnects [86, 87] and other types of passive components (heat spreaders [2, 6]) also face the same main three problems. In this manner, the FET architecture can serve as a potential developmental platform which allows researchers to improve on the mentioned issues while testing devices in required regular operation conditions.

2.4 Conclusions

In conclusion, we summarized and compared the intrinsic-like and extrinsic electrical properties of graphene. More specifically, we examined the physics behind the transfer and output characteristics and explained how detrimental effects, such as charge impurities and series resistance, affect them accordingly. Additionally, we categorized and summarized the most relevant obstacles that hinder development of graphene nano- and macro-electronics. Next we introduced the work, within this framework, that will be presented in Chapters 3, 4, and 5. And finally, we highlighted the flexibility of the graphene FET architecture in order to serve as a developmental platform.

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CHAPTER 3: GRAPHENE HIGH-K INTERFACE NANOSECOND PULSED CHARACTERIZATION

In the previous two chapters we introduced some of the most important graphene physical properties and discussed the fundamental operation and electrical characteristics of graphene based field-effect transistors. Furthermore, we introduced the concept of using a FET structure as a graphene test and developmental platform, since it allows us to measure its electrical properties, while dealing with performance issues (i.e. mainly due to interfaces and contacts) which we are trying to reduce/eliminate. In order for graphene to emerge from a research/experimental phase onto industrial level commercialization, these challenges need to be resolved. With this concept in mind, we devote this chapter to analyzing graphene-dielectric interfaces by using a novel nanosecond pulsed characterization system.

3.1 Graphene/High-κ Interface

In the past few years, practical circuits have been demonstrated using graphene field effect transistors (GFETs), including amplifiers [1, 2], inverters [3], ring oscillators [4], radio-frequency (RF) mixers [5-7] and wafer-scale ICs [8]. However, depending on the high-permittivity (high-κ) top gate dielectric used, the graphene-dielectric interface, and the testing conditions (e.g. air ambient vs. vacuum) GFETs often exhibit characteristics that depend on the voltage sweep direction, i.e. hysteresis (Figure 3.1). The hysteresis shift can be defined as the difference in Dirac voltage (V_0) between forward (FWD) and reverse (REV) gate voltage

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sweeps ($\Delta V_0 = V_{0,FWD} - V_{0,REV}$), where V_0 is the gate voltage of minimum conductivity in the graphene channel (referred to as the Dirac voltage), and can be considered analogous to the threshold voltage in traditional MOSFETs.

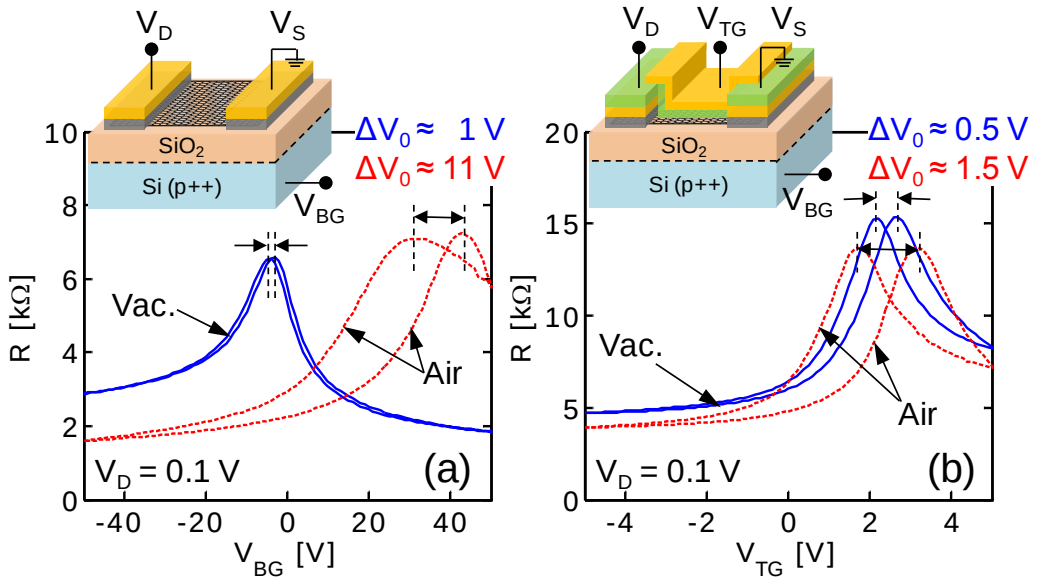

Figure 3.1. Electrical transfer characteristics for a GFET with (a) a 90 nm SiO_2 bottom-gate and (b) a 20 nm Al_2O_3 top-gate (EOT ≈ 13 nm). Note that hysteresis (ΔV_0) for both types of structures is significantly reduced for measurements in vacuum (solid blue lines) compared to in air (dashed red lines). The respective inset in each case shows schematics of the measured structures with channel dimensions: $L \times W = 7 \times 5$ µm.

Hysteresis is primarily caused by charge trapping [9-11] at the graphene-dielectric interfaces and by ambient molecules (i.e. water and oxygen) in contact with the graphene surface [12]. The latter effect can be reduced or eliminated by measurements under vacuum conditions (~10^{-5} Torr) [10, 13], as shown in Figure 3.1(a); this detrimental effect can be reduced even further after an annealing step [13, 14]. However, trapping at the interfaces or within the bulk of the dielectrics surrounding the graphene channel is an inherent and challenging problem [Figure 3.1(b)]. Ultimately, such trapping causes device reliability and operation issues which translate to changes in carrier concentrations, and thus introduce

uncertainties when extracting parameters of interest including mobility, contact resistance, and transconductance. Similar threshold voltage instabilities had also been observed in the early years of silicon technology [15] and as recently as the last decade with the introduction of high-κ dielectrics and metal gate stacks [16, 17]. Addressing such trapping and voltage instability issues is crucial for the continued development and accurate metrology of GFETs.

In this chapter, we investigate the effect of pulsed current-voltage (*I–V*) measurements on the hysteresis and extracted parameters (such as mobility) of top-gated GFETs. Sub-microsecond pulsed output characteristics of top-gated exfoliated graphene FETs [18], and micro- to millisecond pulsed transfer characteristics of back-gated FETs [9, 10, 12] were previously reported (sweep rates used in Ref. [12] range from 0.19 V/s to 4.18 V/s); the latter only probing trapping at the graphene-SiO_2 interface. Here we use graphene grown by large scale chemical vapor deposition (CVD) and examine the gate and drain effects of reducing drain and gate pulse widths down to 75 and 150 ns respectively (more than 5x smaller than the shortest pulses previously investigated [18]). We uncover two apparent trapping time constants of approximately 0.3 and 4.2 μs, ostensibly due to imperfections in the top-gate high-κ dielectric (Al_2O_3), its interface (oxidized Al seeding layer), or the graphene itself. Hysteresis is greatly reduced when using nanosecond voltage pulses at the drain and gate terminals, effectively limiting the time over which charge trapping can occur. The extracted mobility is independent of sweep direction and up to a factor of two higher than if DC measurements were simply employed. The approach described here leads to reliable characterization of GFETs, even in the face of imperfect dielectrics and interfaces.

3.2 Experimental Methods

Graphene is grown on copper foils similarly to our previous work [3, 19], using CVD with a methane/hydrogen mixture as precursor gases. It is then transferred onto SiO_2 (300 nm)/Si substrates using a dual stack of poly(methyl methacrylate) (PMMA) for support and protection (60 nm of 495 A2 and 250 nm of 950 A4). PMMA is removed using a 1:1 solution of dichloride-methane and methanol, followed by a H_2/Ar anneal (2 hours at 400 °C) [20]. Next, Ti/Pd/Au (0.7/20/20 nm) source/drain electrodes are fabricated using UV lithography and e-beam evaporation, followed by O_2-plasma channel definition and atomic layer deposition (ALD) of $t_{ox} \approx 20$ nm of Al_2O_3 (seeded by 1.5 nm of evaporated and oxidized Al). Finally, a Ti/Au (0.7/20 nm) top gate with a gate-source/drain overlap of ~150 nm is fabricated using e-beam lithography. Channel dimensions (L and W) range from 2 – 10 μm.

Figure 3.2 (a) and (b) show the schematic, optical and scanning electron microscope (SEM) images of completed devices. Raman spectra taken after transfer [inset of Figure 3.2(b)] indicate that graphene is monolayer (2D-peak to G-peak integrated intensity ratio $I_{2D}/I_G \approx 2$) and with D-peak to G-peak integrated intensity ratio $I_D/I_G \approx 0.25 \pm 0.15$ [21]. From the I_D/I_G ratio we estimate [22] an average distance between Raman-active defects to be $L_a \approx 250 \pm 150$ nm. Considering micron-scale device dimensions used here, we expect the presence of defects and grain boundaries within the channel [23], and thus lower mobility values than those of exfoliated (single crystal) graphene devices [24].

During measurements, we apply voltage pulses (V_P) at the drain while increasing the amplitude of voltage pulses at the top gate (V_{TG}), as shown in Figure 3.2(c) and (d). The V_D pulse is applied after the rising (t_R) edge and removed before the falling (t_F) edges of V_{TG}, since gate pulse edges cause a small “resonance” on V_D, especially at larger amplitudes (i.e.

V_{TG} > 2 V) and shorter edges ($t_R = t_F$ < 500 ns). Hence, the full-width at half-maximum (FWHM) of V_{TG} is twice that of V_D ($t_{ON,TG} = 2 \cdot t_{ON,D}$) and a delay relative to V_{TG} ($d = t_{ON,D} / 2$) is half the width of V_D [Figure 3.2(e)]. We find that these two constraints maximize signal integrity. The rise (t_R) and fall (t_F) times of gate or drain pulses vary depending on their width (i.e. $t_R = t_F$ = 10 ns for $t_{ON,D}$ = 75 ns and $t_R = t_F$ = 20 – 50 ns for $t_{ON,TG}$ = 150 ns).

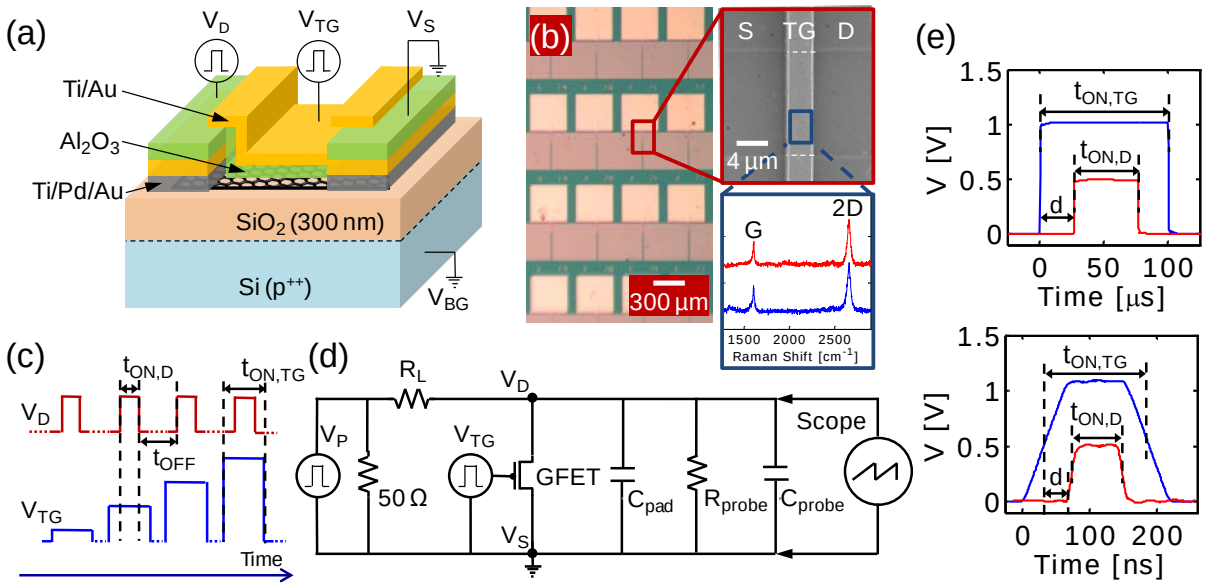

Figure 3.2. (a) Schematic of top-gated graphene field-effect transistors (GFETs) fabricated in this work. (b) Optical, scanning electron microscope (SEM) images, and Raman spectra of typical devices. (c) Schematic of pulses and biases applied at top gate (V_{TG}) and drain (V_D) terminals. The amplitude of V_{TG} is increased when performing a gate sweep of the voltage. (d) Diagram of circuit used to apply voltage pulses at drain and gate terminals. Current is calculated from the voltage drops across load resistor (R_L = 0.5-1.5 kΩ), GFET, probe resistance (R_{probe} = 100 kΩ) and pad (C_{pad} = 8.3 pF) and probe capacitances (C_{probe} = 0.8 pF). (e) Measured drain and top gate pulses –top gate scope connection not shown Figure 3.2(d)– with $t_{ON,TG}$ = 100 µs and $t_{ON,D}$ = 50 µs (top) and $t_{ON,TG}$ = 150 ns and $t_{ON,D}$ = 75 ns. In both cases V_D has a delay $d = t_{ON,D} / 2$ relative to V_{TG}. Also, V_{TG} = 1 V and V_D = 0.5 V.

The off-state relaxation time between drain pulses (t_{OFF}) ranges between 0.1-1 ms, which is 3-4 orders of magnitude larger than shortest $t_{ON,D}$ applied (75 ns). These off-times were found to be sufficiently long to relax all measurable effects of charge trapping from our short pulses. Larger relaxation times (up to the range of seconds) have been used while

studying trapping at the graphene/SiO_2 [9-12] and CNT/SiO_2 [25] interfaces. In contrast, our analysis attempts to study and control trapping by using nanosecond-range top gate pulses ($t_{ON,TG}$) and effectively limiting the amount of carriers than can become trapped, instead of increasing de-trapping via longer off-state relaxation.

In order to measure pulsed *I-V* characteristics we employ a pulse generator, a 1.5-GHz oscilloscope, an active probe and a simple voltage divider circuit in our setup [Figure 3.2(d)]. For each top gate pulse (V_{TG}), a corresponding voltage pulse is applied to a load resistor (R_L), such that after subtracting its voltage drop (V_{RL}), a pulse of amplitude V_D is applied to the GFET ($V_D = V_P - V_{RL}$). For I_D-V_{TG} measurements, the amplitude of V_D is kept the same throughout the measurement by adjusting the amplitude of the pulse V_P at each V_{TG} bias through a feedback loop (since V_{RL} changes with the bias-dependent resistance of the device). Every recorded V_D waveform (at a given V_{TG}) is an average over 200 applied pulses. The time dependence of the drain current I_D(t) is obtained from the voltage drops across the load resistor (R_L) and a 50 Ω matching resistor (in parallel with the 50 Ω output impedance of the pulse generator), the GFET, the active probe resistance (R_{probe}) and pad (C_{pad}) and probe capacitances (C_{probe}), such that:

$$I_D(t) = \frac{V_P(t) - V_D(t)}{R_L + 25\,\Omega} - \frac{V_D(t)}{R_{probe}} - \left(C_{pad} + C_{probe}\right) \times \frac{dV_D(t)}{dt} \qquad \text{Eq. 3.1}$$

3.3 Pulsed Measurements Results

With this setup, we first look at typical transient behavior of current [Figure 3.3(a)] when $t_{ON,D}$ = 50 µs pulses are applied at the drain terminal. I_D reaches steady state with ~10% degradation after ~10 µs due to effect of charge traps at this particular bias condition. This

drop-off is faster than previous reports [9, 12] which studied charge trapping at back gates with much thicker amorphous SiO_2 layers. The best fit of $I_D(t)$ is obtained by using two decaying exponentials of the form $A \cdot \exp(-t/\tau)$ (black dashed lines) yielding time constants τ_1 = 0.3 μs and τ_2 = 4.2 μs. These suggest the presence of at least two trapping mechanisms such as interface and bulk trapping [18, 26, 27]. Interface trap response times scale exponentially with their energy difference from either the valence or conduction bands of a typical channel material [26]. Since graphene does not have a band gap and trap states can be located across a wide range of energies [Figure 3.3(b)], interface traps can be rapidly filled when the energy of carriers is higher than that of electron (x-symbols) or hole traps (circles). On the other hand, bulk trap response times depend on tunneling through the oxide, and thus they are expected to be slower. In our case, the oxidized Al seeding layer (AlO_x) and graphene imperfections (i.e. grain boundaries) could be responsible for contributions to interface trapping, while the ALD grown Al_2O_3 potentially contributes to bulk trapping. Our pulsed technique identifies two time constants (Figure 3.3), likely corresponding to these two processes, but their individual contributions cannot be distinguished further. Also, identifying with certainty the physical nature and location (in the oxide) of these trapped states requires more in-depth analysis and modeling than the results shown in this section.

Furthermore, the time constants identified here (0.3 and 4.2 μs) are not originated from circuit transients, as circuit RC time constants due to R_L, R_{GFET}, R_{probe}, C_{pad} and C_{probe} are ~10 ns. However, thermal time constants of top-gated GFETs with similar geometry are of the order ~100 ns [28], thus it is possible that the shorter time constant found here (τ_1 = 0.3 μs) can include a small thermal self-heating transient, which can also influence current

degradation (although we note that our pulsed measurements were done at relatively low current density, ~0.1 mA/μm, except those in Section 3.6).

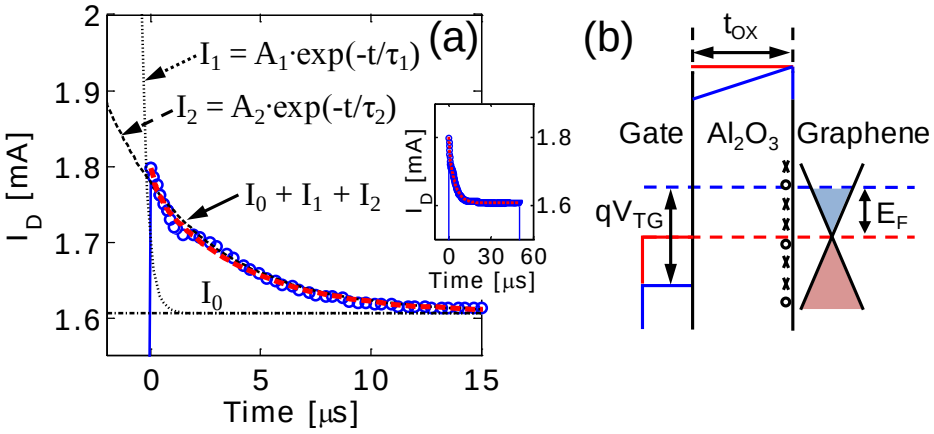

Figure 3.3. (a) Measured drain current ID (blue circles and line) during the first 15 μs of a typical 50-μs pulse (V_D = 1.9 V, V_{TG} = 0.5 V). Inset shows the same data set, zoomed out for the entire 50 μs. Device measured in air ambient, $L \times W$ = 2×10 μm. Transient behavior is due to population of interface and bulk oxide charge traps. Current is fitted (red dashed lines) with as $I_D(t) = I_0 + A_1 \cdot \exp(-t/\tau_1) + A_2 \cdot \exp(-t/\tau_2)$. Exponential terms are shifted by I_0 and shown in black dashed and dotted lines. Fitting parameters are I_0 = 1.6 mA, A_1 = 0.03 mA, A_2 = 0.16 mA, with two time constants τ_1 = 0.3 μs and τ_2 = 4.2 μs. (b) Schematic band diagram of the metal-oxide-graphene device showing population of interface traps as the graphene Fermi level (dashed) increases from qV_0 (red) to qV_{TG} (blue). Interface states could act as either hole (circles) or electron (x-symbols) traps.

The effect of trap filling on electrical measurements can also be seen in [Figure 3.4(a)], where the DC transfer characteristics of a typical top-gated GFET ($L \times W$ = 2×10 μm) show Dirac voltage shift and hysteresis (ΔV_0) in air and in vacuum measurements. Charge trapping (or de-trapping) is less likely to occur at the bottom graphene/SiO_2 interface when we vary V_{TG} as the voltage drop between the graphene and back-gate is small (V_{BG} = 0 V). The presence of hysteresis in both air and vacuum suggests that ambient adsorbates (i.e. O_2, H_2O) and the top dielectric trapping (interface and bulk) contribute to the change in carrier density in the channel while the DC top-gate voltage is swept [9, 10]. Thus, in order to minimize such V_0 instabilities, we perform pulsed measurements as described above. For each V_{TG} bias

I_D is calculated as a function of time using eq. (1) and its amplitude is averaged over the duration ($t_{ON,D}$) of each drain pulse. Figure 3.4(b) displays the in-air transfer characteristics for different V_{TG} on-times ($t_{ON,TG}$) and compares them with simple DC *I-V*s using the same bias conditions (V_D = 0.5 V and V_{BG} = 0 V). As $t_{ON,TG}$ is decreased from 100 µs to 400 ns, forward (FWD) and reverse (REV) sweeps collapse onto one another and hysteresis ΔV_0 disappears. In Figure 3.4(c), the corresponding ΔV_0 is displayed as a function of $t_{ON,TG}$ down to 150 ns; we note that for DC *I-V*s ΔV_0 = 2.3 V, while for $t_{ON,TG}$ < 500 ns hysteresis ΔV_0 approaches 0 V. This ΔV_0 reduction was observed across 20 devices (L, W = 2–10 µm) [Figure 3.4(d)] for five testing conditions: $t_{ON,TG}$ = 0.15, 1, 10, 100 µs and DC. We attribute the broadening of each distribution (corresponding to each $t_{ON,TG}$ case) to device-to-device variations, i.e. graphene quality and contact resistance.

The transfer characteristics shown in Figure 3.4(b) are consistent with the presence of negative charges in the oxide. The fixed negative charges can be present in Al_2O_3 imperfections [29], and are apparent since V_0 > 0 V for all measurements (DC and pulsed) and sweep directions (FWD and REV). The occupied trapped states, responsible for Dirac voltage shift (ΔV_0) and hysteresis, depend on pulse duration; shorter pulses limit the electrical stress time over which carriers can become trapped. We also observe that the (unified) Dirac voltage of the 400-ns pulsed sweep falls between that of the FWD and REV DC sweeps. These differences in V_0 are consistent with hole traps charging up in the oxide (making it less negative) when V_{TG} is swept FWD starting in the hole region (V_{TG} < V_0), and with electron traps accumulating during the REV sweep in the electron region (V_{TG} > V_0) (making the oxide more negative). These additional trapped states in the oxide also contribute to the apparent variation of the channel resistance at V_0 in DC sweeps by

increasing the charge puddle density (i.e. increasing impurity or minimum carrier densities in the channel) [24]. In contrast, when using short pulses (< 1 μs) less trapped states are disturbed and V_0 and $R(V_{TG} = V_0)$ remain constant independent of sweep direction.

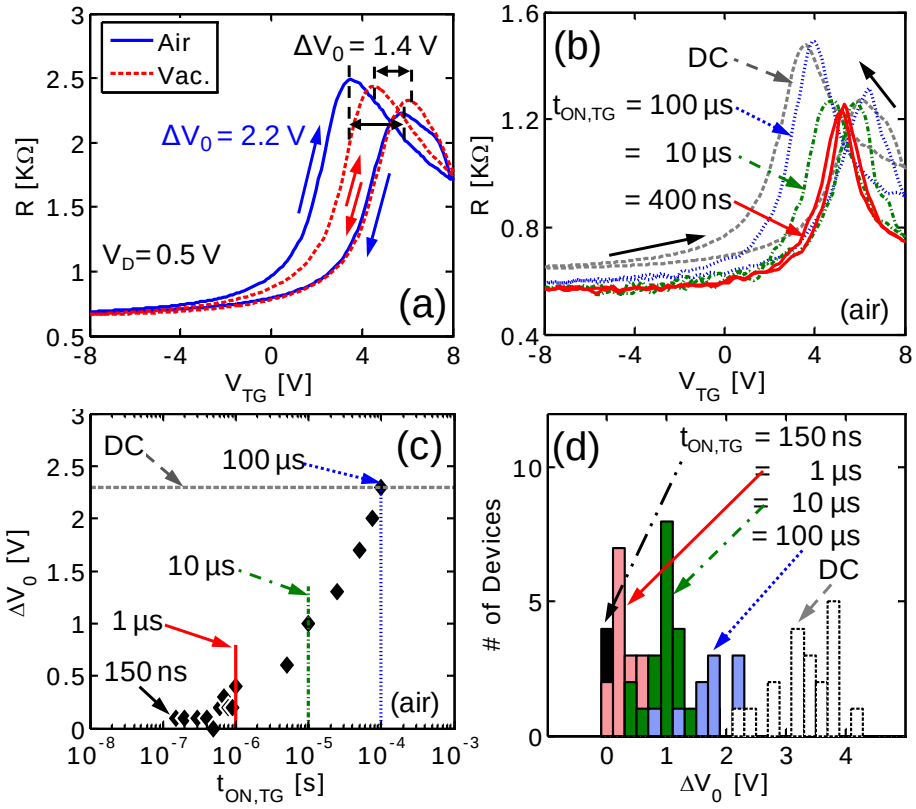

Figure 3.4. (a) Hysteresis in DC measurement of resistance (R) vs. top gate voltage (V_{TG}) of a typical device ($L \times W$ = 4×8 μm) in air (blue-solid) and in vacuum (red-dashed). Arrows indicate sweep directions (from -8 V to +8 V and back). Hysteresis is ΔV_0 = 2.2 V and 1.4 V in air and in vacuum, respectively (V_D = 0.5 V). (b) Typical R-V_{TG} characteristics of another device measured in air under DC (dashed lines) and pulsed conditions. Note the suppression of hysteresis between FWD and REV sweeps as $t_{ON,TG}$ decreases to 400 ns. $L \times W$ = 2×10 μm. (c) Measured shift in Dirac voltage (ΔV_0) from Figure 3.4(b) as a function of $t_{ON,TG}$. ΔV_0 is marked (lines and arrows) at five selected testing conditions: $t_{ON,TG}$ = 0.15, 1, 10, 100 μs and DC (d) Histogram of ΔV_0 for 20 devices measured at same five testing conditions: $t_{ON,TG}$ = 0.15, 1, 10, 100 μs and DC. Note that not all devices were tested for each case.

3.4 Gate Capacitance and Trap Charging Effects

In order to estimate quantitatively oxide trapped charge densities responsible for hysteresis, we examine capacitance through measurements and modeling. First, we estimate the top dielectric capacitance as suggested in [30], by measuring the top-gate Dirac voltage ($V_{0,TG}$) shift as a function of V_{BG}, in vacuum. As shown in Figure 3.5(a), this yields the ratio between the top- and back-gate oxide capacitance, $C_{ox}/C_{BG} \approx 22$ which gives $C_{ox} \approx 250$ nF/cm^2 and $\varepsilon_{ox} \approx 5.7$ for our top Al_2O_3 dielectric with oxidized Al seeding layer. Next, we measure *C*-*V* characteristics [Figure 3.5(b)] by applying DC and AC voltages to the top-gate terminal with an LCR meter. Away from the Dirac voltage, C_{TG} approaches the previously estimated top-layer capacitance ($C_{ox} = \varepsilon_{ox}/t_{ox}$) while near V_0, it decreases and exhibits hysteresis similar to that seen in the *I*-*V* measurements (Figure 3.4). Finally, we fit a *C*-*V* model to obtain trapped charge densities in the top gate dielectric stack quantitatively. Gauss' law applied to our structure gives:

$$V_{TG} - \left[V_0 + \frac{Q_{it}\left(E_F = 0\right)}{C_{TG}} \right] = -\frac{\left[Q_n\left(E_F\right) + Q_{it}\left(E_F\right) \right]}{C_{TG}} + \frac{E_F}{q} \qquad \text{Eq. 3.2}$$

where E_F is the Fermi level in graphene [Figure 3.3(b)], Q_n is the charge density in graphene and Q_{it} is the sum of trapped charge accumulated at the AlO_x/graphene interface and Al_2O_3 bulk. Quantum capacitance (C_q) is included in our model explicitly in the carrier density [$Q_n(E_F)$] calculation by integrating over the density of states. The total capacitance (C_{TG}) is calculated [Figure 3.5(b)] as a derivative of the total charge ($Q_{TG} = Q_n + Q_{it}$) to the gate voltage by varying E_F, such that

$$C_{TG} = \left(\frac{\partial Q_{TG}}{\partial E_F}\right)\left(\frac{\partial V_{TG}}{\partial E_F}\right)^{-1} \qquad \text{Eq. 3.3}$$

From this model we extract trapped charge densities of -7.2 × 10^{11} cm^{-2} and -10^{12} for the FWD and REV sweeps, respectively, at E_F = 0 eV (Dirac point).

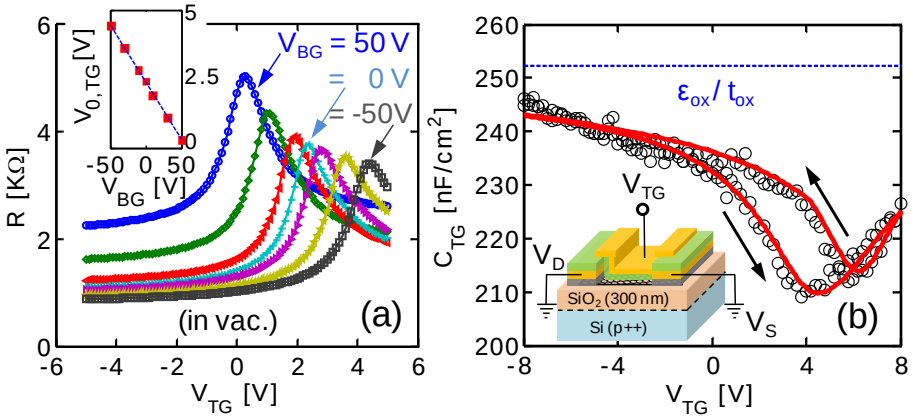

Figure 3.5. (a) DC R-V_{TG} for different V_{BG} values. L×W = 5×5 μm, V_D = 0.1 V only forward sweep shown. (Inset) $V_{0,TG}$ vs. V_{BG}. Slope represents ratio between top and back-gate oxide capacitances ($C_{ox}/C_{BG} \approx 22$). (b) Measured top-gate capacitance at 100 kHz (C_{TG}, circles) and calculated (red solid line) using model described in text. Expected value from simpler extraction in (a) is also shown (dashed line). Inset shows schematic of measurement. V_{TG} is applied to top-gate, source/drain are grounded and back gate is left disconnected. Side-wall and overlap capacitances which appear in parallel with C_{TG} were measured in similar FET structures without graphene, and subtracted from the result.

3.5 Pulsed Mobility Extraction

Next, we extract device transconductance (g_m) and effective hole mobilities (μ_h) from pulsed and DC measurements [Figure 3.4(b)]. We do so by first fitting a transport model (R_{fit}) [24, 31], which includes contact resistance ($R_C \approx 2$–3 kΩ·μm), to the measured I_D–V_{TG} characteristics (R_{meas}) as shown in Figure 3.6(a). Figure 3.6(b) then displays the *intrinsic* transconductance g_m' (calculated after R_C is subtracted) derived from 400-ns pulsed

measurements (red) and DC measurements (black) for FWD and REV sweep directions. We note that g_m' changes sign as V_{TG} is swept past the Dirac point (i.e. threshold voltage) and carrier transport changes from holes to electrons. Also hysteresis is greatly reduced with 400 ns pulses compared to the DC measurement. Furthermore, the maximum value of g_m' for pulsed measurements (~100 μS/μm) is approximately twice as high as the one obtained from DC measurements (~50 μS/μm). This trend is evident from the inset of Figure 3.6(b), which shows the maximum g_m' (from FWD sweep) as a function of gate on-time. Note that extrinsic transconductance values (g_m) were smaller by about a factor of five.

In Figure 3.6(c) we display the effective mobility calculated as in Refs. [24, 31]. We note that mobility values are approximate since R_C is fitted and not directly measured. Additionally, we used C_{ox} in our fitting transport models since measured C_{TG} includes frequency dependent trap capacitance components, which could complicate carrier density extraction for each pulsed case. Nevertheless, this exercise illustrates the consistency and reliability of pulsed characterization vs. DC measurements. We show hole mobility (μ_h) vs. carrier density for 400 ns pulses (red) and DC measurements (black), from FWD and REV sweeps. Pulsed measurements generate higher and consistent mobility values, due to reduced charge trapping. Conversely, mobility appears to be a function of sweep direction (marked with arrows) when obtained from DC *I-V* measurements. We note that self-heating effects do not play a role because the mobility estimates are all done at low lateral field and low current levels, ~0.06 mA/μm, where the maximum temperature rise is at most 5 K for our GFETs [24, 28], even for the DC measurements.

Subsequently, we examine mobility dependence on $t_{ON,TG.}$ Figure 3.6(d) shows μ_h at three carrier densities: 0.7, 1, and 5×10^{12} cm^{-2}; open circles and solid diamonds represent

values from FWD and REV sweeps. The mobility range from DC measurements (top and bottom lines of shaded regions) has an uncertainty up to 1000 $cm^2V^{-1}s^{-1}$ (or ~30%), while for pulsed characterization this uncertainty is significantly smaller (~50 $cm^2V^{-1}s^{-1}$ or ~2%). Once again, we note that mobility is higher at shorter pulses, due to the minimized trapped charge.

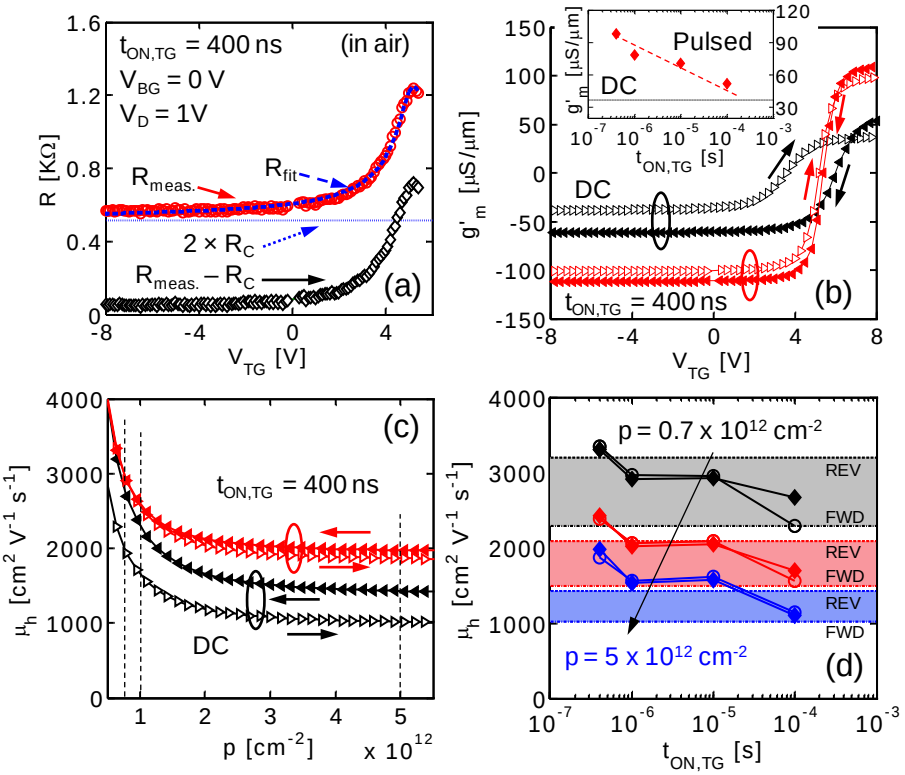

Figure 3.6. (a) Hole R-V_{TG} measured (R_{meas}), fitted (R_{fit}) as in Ref. [31] and with contact resistance (R_C) subtracted (R_{meas}–R_C). (b) Intrinsic trans-conductance (g_m') from Figure 3.4(b), as a function of V_{TG} from pulsed (red) ($t_{ON,TG}$ = 400 ns) and DC (black) measurements. Arrows indicate direction (FWD or REV) of sweep. Inset shows maximum |g_m'| (from FWD sweeps) as a function of gate on-times. (c) Extracted hole mobility as a function of carrier density (p) from Figure 3.4(b). (d) Hole mobility vs. $t_{ON,TG}$ for different p = 0.7 (black), 1 (red), and 5×10^{12} cm^{-2} (blue). Values extracted from Figure 3.6(c) at the marked (vertical dashed lines) concentrations. Open circles and solid diamonds are from FWD and REV pulsed sweeps respectively. Values extracted from DC FWD and REV sweeps mark limits of shaded regions. Note large mobility uncertainty of DC sweeps (up to ~1000 $cm^2V^{-1}s^{-1}$ or ~30 %) compared to pulsed sweeps (~50 $cm^2V^{-1}s^{-1}$ or ~2 %).

3.6 High Field Effects

We also briefly examine the effects of high lateral *intrinsic* fields F_x' (after subtracting R_C) on ΔV_0 by using our nanosecond pulsed technique. First, we find that for F_x' ~ 0.1 V/μm and a constant $t_{ON,TG}$ (3 μs), ΔV_0 remains constant as we decrease $t_{ON,D}$ from 2 μs down to 100 ns [Figure 3.7(a)]. Conversely, when we raise F_x' to 0.5 V/μm, ΔV_0 drastically increases as well. This increased ΔV_0 caused by higher F_x' occurs when hot carriers in the channel begin to fill interface or bulk trap states of the dielectric [18]. Finally, we examine ΔV_0 as we decrease $t_{ON,TG}$ and replace the pulse generator at the drain terminal with a regular DC supply. We find that, at low F_x', ΔV_0 is equally suppressed by using a pulsed or a DC voltage at the drain terminal [Figure 3.7(b)].

In general, GFETs hysteresis is a function of the amount of trapped charge at the interface and bulk of the dielectric (Q*it*), which in turn affects the overall charge in the channel, capacitance and ultimately *I*-*V* results. Also, Q*it* is a function of frequency, gate voltage (V_{TG} or V_{BG}) and intrinsic lateral field (F_x'). Thus, in order to eliminate hysteresis and Dirac voltage instabilities during measurements, one should take into account these dependencies and bias devices accordingly.

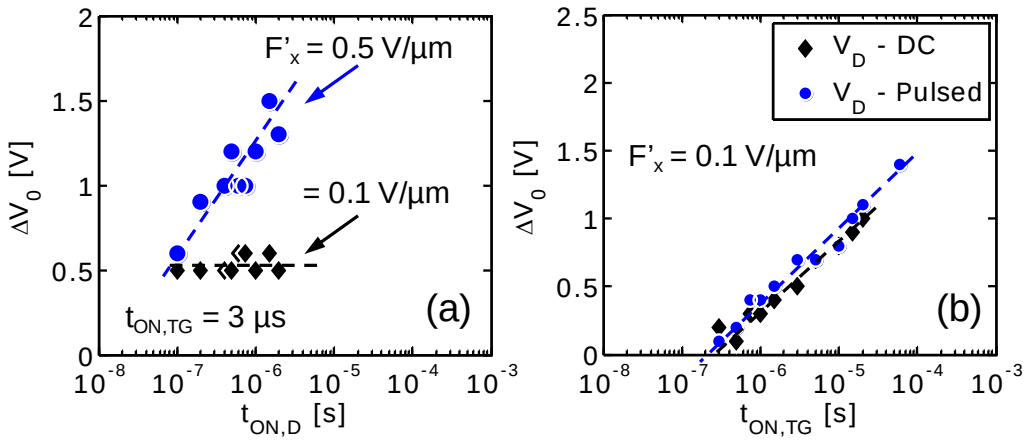

Figure 3.7. (a) Dirac voltage shift (ΔV_0) as a function of drain on-time ($t_{ON,D}$ = 100 ns to 2 µs and $t_{ON,TG}$ = 3 µs). The V_{TG} sweeps (not shown) are from -8 V to 8 V and back to -8 V, while V_D is increased from 1 V (black diamonds) to 3 V (blue circles). V_D values correspond to intrinsic lateral fields $F_x' \approx 0.1$ and 0.5 V/µm, respectively, after contact resistance is subtracted ($L \times W$ = 3×9 µm). (b) ΔV_0 vs. $t_{ON,TG}$ (300 ns to 80 µs). The drain terminal is biased using a DC (diamonds) and pulsed bias (circles) (F_x' = 0.1 V/µm , $t_{ON,D} = 0.5 \cdot t_{ON,TG}$).

3.7 Conclusions

In conclusion, intrinsic properties of GFETs can be probed with pulsed operation and pulses shorter than the trapping time constants of interface and bulk trapping. We also report transfer characteristics, transconductance and mobility values that do not depend on voltage sweep direction (forward or reverse) or rate. Such results "correctly" represent the *intrinsic* properties of the GFET channel, as detrimental effects from oxide and interface traps (hysteresis and I_D degradation) can be greatly reduced. Finally, we show that high lateral fields can affect hysteresis and charge trapping through hot carrier injection, a situation that can also be mitigated by using short drain on-times. All of these findings shed light on careful ways to characterize graphene devices and reduce detrimental effects by using pulsed measurements, which is important for future advancement of graphene device technology.

3.8 References

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CHAPTER 4: VARIABILITY OF GRAPHENE MOBILITY AND CONTACTS: SURFACE EFFECTS, DOPING, AND STRAIN

Another important and necessary issue to overcome when it comes to development of graphene electronics is the significant device-to-device variability. All large-area implementations require the ability to fabricate wafer-scale graphene with optimized, reliable, and reproducible electrical characteristics. To this end, chemical vapor deposition (CVD) can be used to grow large-scale graphene on Ni [1], Cu [2] and Ge [3] substrates. However, such graphene most often requires transfer from the initial catalyst to other insulating substrates using a sacrificial polymer scaffold, and as a result the graphene properties exhibit substantial electrical variability [4]. Furthermore, while much effort has been devoted to improving electrical characteristics through substrate engineering [5-7], high-k dielectric scaling [8, 9] and graphene surface treatments and anneals [4, 10, 11], the fundamental physical sources of the electrical variability in polymer transferred graphene and how they might be controlled or minimized remain poorly understood.

In this chapter, we methodically investigate variability of contact resistance and mobility in GFETs fabricated with CVD graphene transferred to SiO_2/Si substrates using three polymer scaffolds: PMMA, poly(bisphenol A carbonate) (PC), and a PC/PMMA bilayer (PC being in contact with graphene). In general, by extensive analysis of hundreds of Raman spectra, we find that the polymer-graphene mechanical and chemical (via charge transfer) interaction, as well as the presence of surface residues, induce changes in graphene

surface roughness (up to ~0.2 nm), doping concentrations (up to ~2×10^{12} cm^{-2}), and strain levels (up to ~0.2%) depending on which polymer transfer layers and annealing conditions (i.e. temperature and time) are used. We uncover that the PC/PMMA scaffolds yield a combination of (low) spatially uniform strain and homogeneous hole doping, which lead to the lowest variability of contact resistance (R_C) and mobility (μ) among the devices investigated.

4.1 Role of Variability

The importance of thorough characterization of electrical variability is two-fold. First, it enables better understanding of intrinsic and extrinsic processes responsible for device-to-device variation, which is necessary to improve the uniformity and reliability of GFETs. Second, it allows assigning quantifiable measures and ranges to variable electrical parameters (i.e. R_C and μ). These parameters can then serve as key inputs for compact models [12, 13], as researchers begin to simulate and develop complex, practical, and realistic graphene-based architectures. Furthermore, the characterization of variability is important in order to develop new systems that could account for errors and variability from a statistical and stochastic point of view. Such systems could open the design space for device engineers, and new types of functionality could be achieved even with GFETs that exhibit some degree of variability. Lastly, we note that large variability issues are not unique to graphene electronics, and they have also posed an increasing challenge in conventional CMOS devices [14].

4.2 Growth and Transfer Process

Our graphene samples are grown on Cu foils using a CVD technique similar to our previous work [15] with detailed description provided in Ref. [16] and in Appendix A. Graphene is then transferred onto SiO_2(90 nm)/Si(p++) substrates [Figure 4.1(a-d)] by a common wet transfer technique and different polymer scaffolds to provide mechanical support and protection: PMMA ≈ 290 ± 10 nm, PC ≈ 70 ± 20 nm, and PC/PMMA ≈ 295 ± 10 nm. After the transfer, each polymer stack is respectively removed as described in Ref. [16] Samples are then annealed in a H_2/Ar flow to remove remaining polymer residues (T = 400 °C, t = 2 h); however even this anneal does not yield a residue-free graphene surface [17, 18]. Finally, we fabricate transistors with photolithography by depositing Pd/Au (20/25 nm) source/drain contacts and defining graphene channels (length, L = 2 − 20 µm and width, W = 5, 10 µm).

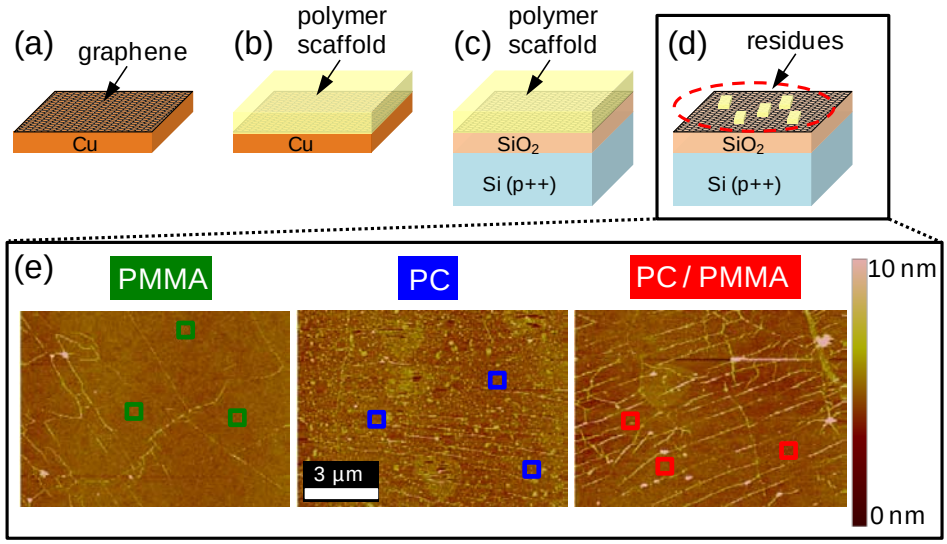

Figure 4.1. (a-d) Process flow of polymer-assisted wet-transfer technique. (e) AFM scans of graphene on SiO_2 transferred using three different polymer scaffolds: PMMA (left, green), PC (middle, blue) and PC/PMMA (red, right) after H_2/Ar anneal (T = 400 °C, t = 2 h). Colored squares (~0.5 × 0. 5 µm^2) mark wrinkle-free regions.

Figure 4.1(e) shows atomic force microscopy (AFM) scans of the graphene surface immediately after transfer with the three polymer scaffolds, confirming the presence of residues and wrinkles in all cases. We note that PC and PC/PMMA polymer stacks produce graphene wrinkles oriented along a preferential direction while the PMMA scaffold yields randomly oriented wrinkles. This could be due to a slightly smaller Young modulus in the PMMA scaffold compared to the PC or the PC/PMMA stacks and it is likely related to the different polymerization mechanisms for PMMA (chain-growth) and PC (step-growth). Furthermore, the root-mean-square (RMS) surface roughness in wrinkle-free regions, marked by $0.5 \times 0.5\ \mu m^2$ squares in Fig. 1(e), is h_{RMS} = 0.19 nm, 0.37 nm, and 0.21 nm for the samples transferred with PMMA, PC, and PC/PMMA scaffolds respectively. Similar surface morphologies are indicative of comparable amounts of leftover polymer residues, which in turn can behave as surface impurities limiting R_C and μ and affecting their variability. We note that in wrinkle-free regions, thicker polymer scaffolds (~300 nm) such as PMMA and PC/PMMA yield similar $h_{RMS} \approx 0.2$ nm, while the thinner (~70 nm) PC film yields h_{RMS} higher by about a factor of two; thus, we expect more of impurities and slightly worse electrical characteristics for PC-transferred graphene.

4.3 Raman Spectroscopy Measurements

Next we examine Raman spectra (Figure 4.2) for the PMMA, PC, and PC/PMMA transferred cases. Figure 4.2(a) shows the well-known 2D, G, and (small) D peaks [19] along with respective Lorentzian fits (black dashed lines) described in more detail in (b), which shows a representative 2D-to-G integrated intensity (I_{2D}/I_G) map for the PC/PMMA case indicating monolayer graphene [20]; the other cases also yield $I_{2D}/I_G \approx 5.0 \pm 0.5$ and are

shown in Figure 4.3 along with the respective values for full-width-at-half-maximum. Figure 4.2(c-f) compare shifts in 2D (ω_{2D}) and G (ω_G) peak position of each transferred case before and after an extended vacuum anneal process (T = 300 °C, t = 15 h, P = 10^{-5} Torr). We note that in our case, the vacuum annealing time is significantly longer (>10 h) than in other studies [4, 17, 21] (1 to 3 h) which use similar temperatures and pressures. This process was carried out after device fabrication in order to aggressively attempt to improve the graphene/metal interface while simultaneously removing polymer residues from the graphene surface. Additionally, in some cases (PMMA Mod.) we used a modified vacuum anneal (T = 200 °C, t = 2 h, P = 10^{-5} Torr) for the PMMA transfer case in order to prevent any possible graphene damage or oxidation.

First, we comment on Raman peak positions *before* extended annealing, as shown in Figure 4.2(c) and (d), using the PMMA-transferred sample as a reference (ω_G = 1603.7 ± 0.8 cm^{-1} and ω_{2D} = 2652.5 ± 1.3 cm^{-1}). By comparison, the PC-transfer G peak is slightly blue-shifted (+1.0 cm^{-1}) and the PC/PMMA is red-shifted (-2.1 cm^{-1}). The 2D peak for the PC transfers is significantly blue-shifted (+4.9 cm^{-1}) but the PC/PMMA case is almost the same (-0.7 cm^{-1}) as the reference with PMMA alone. *After* the extended vacuum anneal, as shown in Figure 4.2(e) and (f), the G peak red-shifts drastically for all cases (-9.4 to -12.5 cm^{-1}) in a similar manner to previous reports[17]. By comparison, the 2D peak red-shifts for PMMA (-3.1 cm^{-1}) and for PC (-1.5 cm^{-1}) and remains almost unchanged for PC/PMMA (+0.7 cm^{-1}). Peak position values for all cases are shown in Table B.1 of Appendix B. The different 2D and G peak position shifts for samples transferred with each polymer scaffold correspond to changes in hole doping concentration (p) and strain level (ε), and are due to the mechanical and chemical interactions of the graphene/polymer interface during transfer. However, the G

and 2D peak position dependencies with a respective level of doping or strain are intrinsically coupled, making it difficult to distinguish and quantify their individual contributions. In the next section, we expand even further on the nature of this strain and doping coupling of Raman measurements and we present a vector model capable of dealing with this limitation.

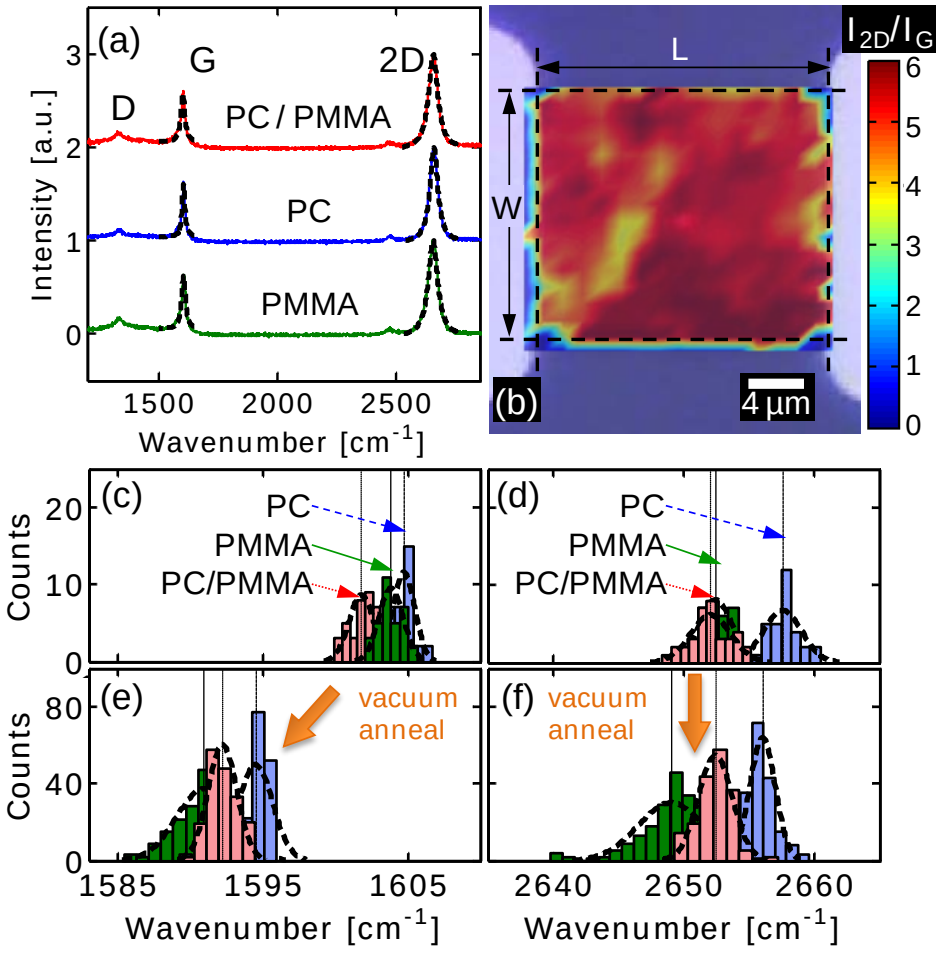

Figure 4.2. (a) Representative Raman spectra for graphene transferred using different polymer scaffolds. Lorentzian fits (black dashed lines) for the 2D and G bands also shown. (b) Representative map of integrated intensity of 2D-to-G ratio. (c) G and (d) 2D band peak position histograms before (top) and after extended vacuum annealing (bottom) for each transferred case.

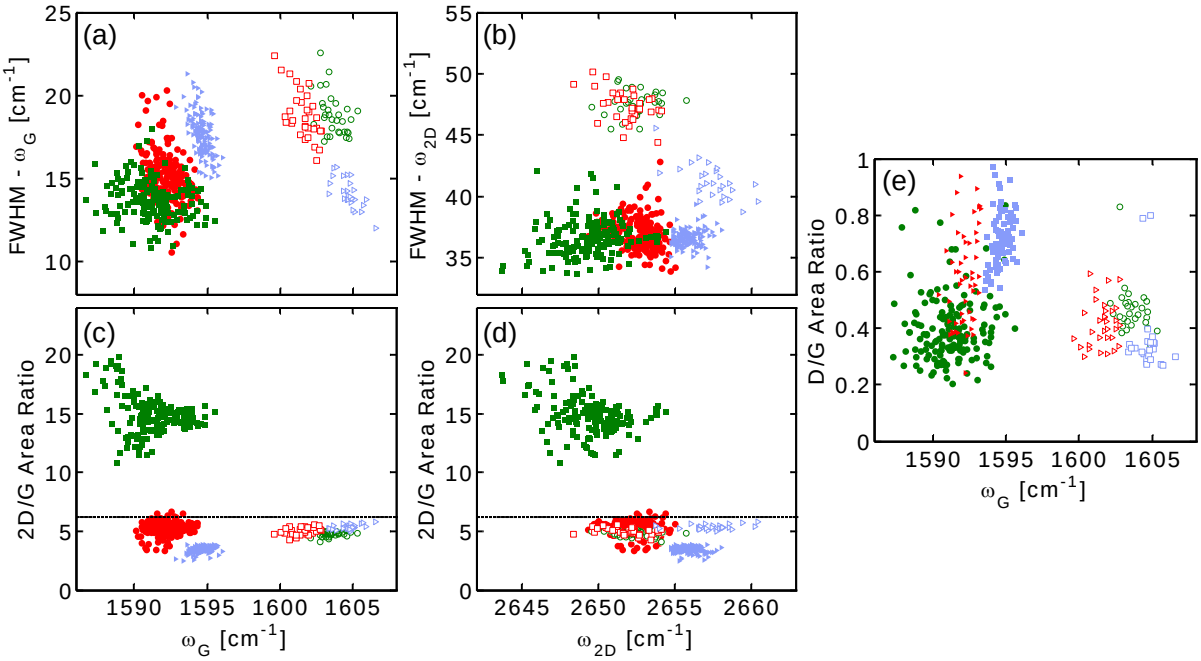

Figure 4.3. (a-b) FWHM, (c-d) 2D/G area ratio from Lorentzian fitting of G and 2D bands as a function of G (ω_G) and 2D (ω_{2D}) peak positions and (e) G/D area ratio vs. G peak position before (open symbols) and after (solid symbols) vacuum annealing for the three polymer scaffolds used: PMMA (green triangles), PC (blue circles), and PC/PMMA (red squares). 2D/G area ratios (dashed lines) for monolayer exfoliated graphene from Ref. [20] also shown.

4.4 Strain and Doping Separation and Vector Model

In general, doping and strain affect the position of the G and 2D bands in a convoluted manner as shown in Figure 4.4. Increased electron or hole doping causes the G peak position to blue-shift while the 2D peak blue-shifts (red shifts) with hole (electron) doping as measured and theoretically predicted [22, 23]. In the case of strain in CVD graphene [24] the G and 2D bands blue-shift (red-shift) with tensile (compressive) strain, in an opposite manner to exfoliated (single-crystal) graphene. These convoluted dependencies prevent us from making quantifiable assertions regarding strain and doping by simply examining changes in the G and 2D peak positions presented in Figure 4.2.

In contrast, in this work we adapt and use a Raman vector model technique first introduced by Ref. [20] to separate and quantify strain and doping contributions by examining graphene Raman data in the ω_G–ω_{2D} space. In order to reproduce such vector model we account for three factors: A) Raman data from a graphene sample with negligible doping and strain contributions, B) the fractional variations of the G and 2D bands ($\Delta\omega_{2D}/\Delta\omega_G$) affected by either doping or strain, and C) the individual dependencies for ω_G and ω_{2D} with doping and strain. The values used here and in Ref. [20] are summarized and compared in Table B.1.

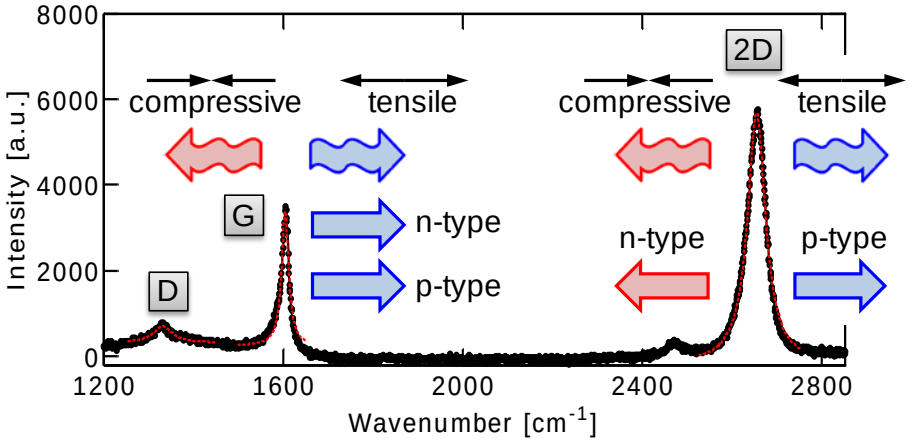

Figure 4.4. G and 2D peak position dependencies with type of doping (*n*- and *p*-type) and strain (compressive and tensile) for CVD grown graphene. All colored arrows point in the direction in which the corresponding band (G or 2D) shifts based on the type of doping (straight arrows) or strain (curved arrows). Red and blue arrows indicate a red- and blue-shift respectively.

A. Origin point: We use Raman data from exfoliated and suspended graphene samples (Figure B.1) similar to Ref. [25]. Exfoliated and suspended graphene over circular trenches (7 µm in diameter), can be considered to have negligible doping concentration (~2×10^{11} cm^{-1}) and strain levels (~0.01 %) [20] due to its intrinsic nature. We average G and 2D frequencies of 15 spectra collected and obtain ω_G^0 = 1583.8 ± 0.6 cm^{-1} and ω_{2D}^0= 2639.5 ±

1.2 cm^{-1}. We obtain different values than those measured in Ref. [20] (ω_{2D}^{0} = 2676.9 ±0.7 cm^{-1}) since the 2D band peak position is strongly dependent on laser excitation energy [26] (this work: 633 nm, Ref. [20]: 514 nm). We note that our averaged measurements (cyan star) fall within theoretical predictions [26]. Finally, we note that theoretically the G band does not depend in laser excitation energy [27], thus we expect and observe that the ω_{G}^{0}measured in this work is similar to the one in Ref. [20].

B. <u>*Strain and Doping Fractional Variations*</u>: The fractional changes of the 2D and G modes ($\Delta\omega_{2D}/\Delta\omega_{G}$) can be quite different from one another due to changes in strain level and doping concentration [20], thus allowing us to separate their relative contributions. In our model, we use the fractional variation values with respect to strain ($\Delta\omega_{2D}/\Delta\omega_{G}|_{\varepsilon}$ = 2.2 ± 0.2) and hole doping ($\Delta\omega_{2D}/\Delta\omega_{G}|_{p}$ = 0.7 ± 0.05) from Ref. [20] since these relative changes are not expected to be affected by the different laser excitation energy used.

C. <u>*Strain and Doping Sensitivity*</u>: We use the strain sensitivity of the G mode ($\Delta\omega_{G}/\Delta\varepsilon$) and the hole doping sensitivity of the 2D mode ($\Delta\omega_{2D}/\Delta p$) in a similar manner as in Ref. [20] to define strain levels and doping concentrations in the ω_{G} vs. ω_{2D} space. In the case of strain we use a sensitivity (41.1 cm^{-1}/%) reported by Ref. [24]. This value drastically differs from the (single crystal) exfoliated graphene case [28] due to the effect of domain boundaries in (polycrystalline) CVD graphene. In the case of hole doping, we use a sensitivity measured and theoretically predicted by Das [22, 23]. Ultimately, by taking into account the three mentioned factors we modified the Raman vector model presented in Ref. [20] and quantify and decouple doping and strain changes.

From this analysis, we find that all samples exhibit certain level of spatial variation in their G and 2D peak positions, resulting in different levels of doping and strain. *Before* the

vacuum anneal (Figure 4.5), graphene transferred with PC (blue triangles) and PC/PMMA (red circles) scaffolds exhibits similar average hole doping concentrations (p = 12.6 ± 0.0 × 10^{12} cm^{-2} and 12.1 ± 0.2 × 10^{12} cm^{-2} respectively) while the graphene from PMMA (green squares) transfers yields p = 13.8 ± 0.2 × 10^{12} cm^{-2}. On the other hand, PC/PMMA and PMMA based transfers exhibit similar and negligible strain levels ($\varepsilon \approx$ 0.00 ± 0.01 % and -0.02 ± 0.01 % respectively) while PC scaffolds lead to a noticeably increase of tensile strain ($\varepsilon \approx$ 0.06 ± 0.02 %). These trends indicate that 1) the PC/graphene interaction does not affect hole doping in graphene as strongly as PMMA does, and 2) the thin PC (~70 nm) scaffold introduces non-negligible graphene strain during transfer. Considering these two factors, the PC/PMMA scaffold seems to be better suited for graphene transfers than PC or PMMA alone. We note that in the PC/PMMA case, the PMMA layer simply provides additional thickness to the scaffold, thus increasing its mechanical rigidity and lowering strain applied to graphene during transfer. However, since the PMMA in this bilayer is not in contact with the graphene (the thin PC is), it does not affect the hole doping as when this scaffold is used alone.

After the extended vacuum anneal (Figure 4.5), p-type doping decreases drastically (Δp = -9.2 to -11.0 × 10^{12} cm^{-2}) due to the further removal of polymer resides from the graphene surface [17, 21]. This decrease is consistent with the Dirac voltage shift (~20 V) measured after the anneal. On the other hand, tensile strain increases ($\Delta\varepsilon \approx$ 0.09 to 0.12 %) with higher temperatures, consistent with G band phonon softening, and domain rotations and slippages [24]. Furthermore, since all samples underwent the same processing steps except for the type of polymer scaffold used, we attribute differences in doping and strain directly to different types and amounts of residue left on the graphene surface, and the polymer-graphene

mechanical and chemical interactions. All of these three factors induce strain and doping, which ultimately modify the graphene Fermi level (E_F).

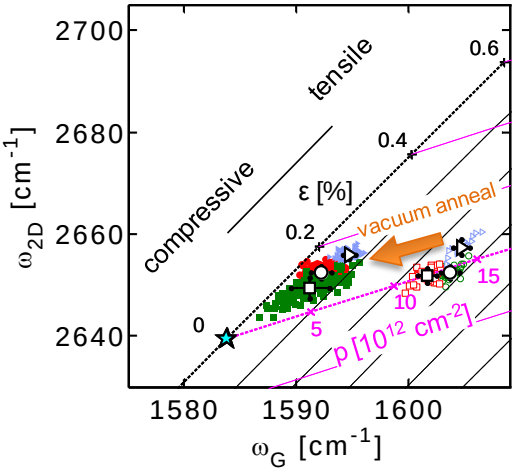

Figure 4.5. G vs. 2D peak positions for graphene transferred using different polymer scaffolds before and after the extended (t = 15 h) 300℃ vacuum anneal: PMMA (green squares), PC (blue circles), and PC/PMMA (red squares). We also show vector model (adapted from Ref. [20]) used to extract and separate contributions from doping (pink axes) and strain (black axes). Open symbols in each case represent average values with respective error bars.

4.5 Electrical Characteristics and Variability

Next we examine the electrical characteristics of GFETs that were transferred using each of the polymers scaffolds described earlier. Figure 4.6(a) shows electrical transfer characteristics (R vs. V_{G0}, where V_{G0} denotes the gate voltage V_G shifted by the Dirac voltage V_0, such that: $V_{G0} = V_G - V_0$) of representative devices for each transferred case *before* vacuum anneal (PMMA: green squares, PC: blue triangles, and PC/PMMA: red circles). We use a transport model [29] (black solid lines) to fit the measurements, extracting contact resistance R_C (dashed color lines), impurity charge density (n_0), and a separate mobility (μ_n, μ_p) for electron and hole regimes, respectively. These fitted and extracted values are

dependent on the measured transport data only, and not on initial fitting parameters used as input. Additionally, we calculate effective mobility (μ_{eff}) as in Ref. [30]. We note that the difference between μ_n or μ_p and μ_{eff} is typically less than 5% (confirming the validity of our extracted results); henceforth, we simply report effective mobility values with the symbol μ_n or μ_p. Additionally, we observe that for all carrier densities R_C is slightly higher for the PMMA and PC scaffolds compared to the PC/PMMA case. This increase is also evident in the output characteristics in Figure 4.6(b) where the highest drive current is measured for the PC/PMMA-transferred device. Figure 4.6(c) shows effective hole mobility (μ_p) as a function of hole concentration (p) for the three cases.

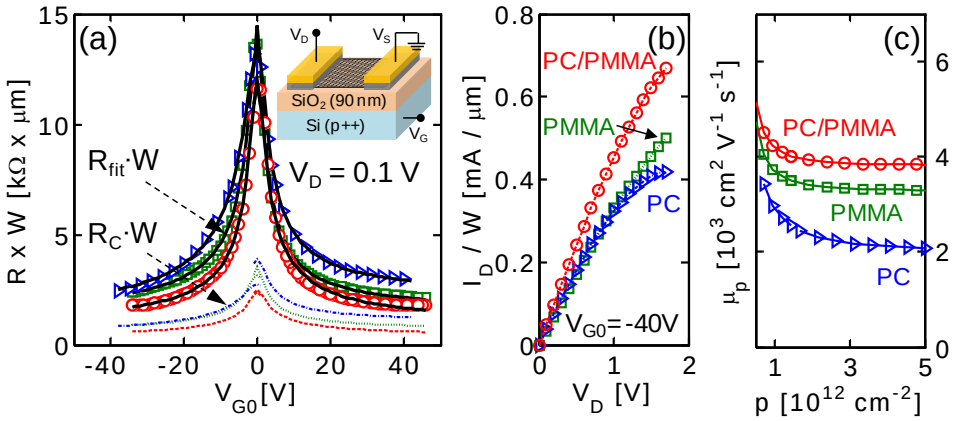

Figure 4.6. Measured (symbols) and fitted (black solid lines) (a) transfer and (b) output characteristics for GFETs transferred using different polymer scaffolds: PMMA (squares), PC (triangles) and PC/PMMA (circles). (c) Hole mobility vs. hole density. $V_{G0} = V_G - V_0$. L = 2 μm, W = 5 μm.

Figure 4.7 shows box plots illustrating the values and variability of electron and hole R_C and μ for over 60 GFETs before (open symbols) and after (closed symbols) undergoing two types of vacuum annealing: *extended* (T = 300 °C, t = 15 h, P = 10^{-5} Torr) and *modified* (T = 200 °C, t = 2 h, P = 10^{-5} Torr). Before this process, the hole R_C is slightly smaller than the electron R_C for all transferred cases, indicating that the Pd Fermi level could be pinned

inside the graphene valence band, leading to improved hole contacts. In addition, we note that the average R_C for both electrons and holes is smaller for GFETs from PC/PMMA (red open circles) transfers compared to the PC (blue open triangles) or PMMA (green open squares and diamonds) cases as shown in Figure 4.7(a-b). This R_C reduction is likely due to a combination of a relatively "clean" surface in wrinkle-free regions and an optimum doping level obtained when using the PC/PMMA scaffold.

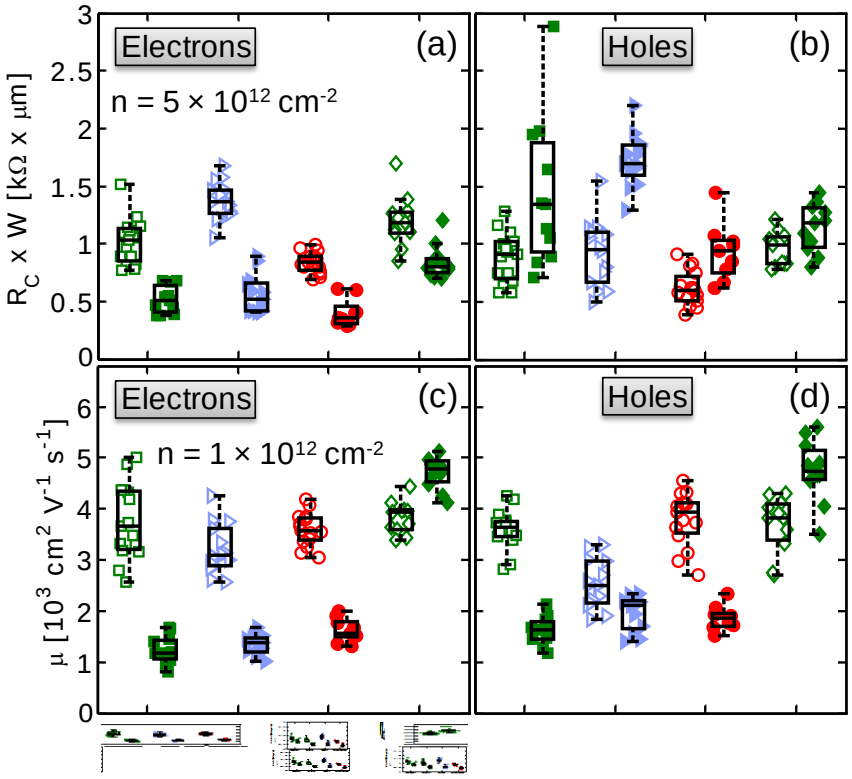

Figure 4.7. Extracted R_C (a-b) and μ (c-d) for electrons and holes for the three types of polymer scaffolds used to transfer graphene which underwent an extended vacuum anneal (T = 300 ^{o}C, t = 15 h, P = 10^{-5} Torr): PMMA (green squares), PC (blue triangles) and PC/PMMA (red circles). Empty and solid symbols represent samples before and after vacuum annealing respectively. Additionally, R_C and μ for devices transferred with PMMA and exposed to the modified vacuum anneal (T = 200 ^{o}C, t = 2 h, P = 10^{-5} Torr) are also shown (green diamonds). Middle of each box denotes the median of respective distributions while top and bottom lines represent 25th and 75th percentiles. Note that average value and overall variability of R_C and μ depends greatly on polymer scaffold and annealing condition used. L = 2, 3 μm, W = 5, 10 and 20 μm.

For the former, a graphene surface roughness ($h_{RMS} \approx 0.21$ nm) comparable to that of the SiO_2 substrate ($h_{RMS} \approx 0.17$ nm), indicates few polymer residues present, thus reducing their effect as scattering impurities or increasing the metal/graphene physical separation. In the latter case, the smaller average doping level obtained with the PC/PMMA scaffold (~12.0 $\times 10^{12}$ cm^{-2}) relative to the PMMA case (~14.0 $\times 10^{12}$ cm^{-2}) indicates a shift in graphene E_F as seen Figure 4.8. This shift could be partially responsible for the improved R_C as the difference between metal work function and graphene E_F decreases. We note that the doping levels reported are obtained from Raman data of exposed graphene channels. Graphene under Pd metal contacts might behave differently due to interactions with the metal (i.e. Fermi level pinning, metal induced doping, sheet resistivity changes, etc.), making it difficult to accurately measure and point out which specific physical factors are responsible for the reported R_C reduction.

In a similar manner as before, Figure 4.7(c-d) shows electron and hole mobility values before (open symbols) and after vacuum annealing (closed symbols). Before the vacuum anneal, the average graphene electron mobility for all scaffolds is somewhat similar ($\mu_n \approx$ 3600 $cm^2V^{-1}s^{-1}$), while the graphene hole mobility is greater for the PMMA ($\mu_p \approx 3650$ $cm^2V^{-1}s^{-1}$) and PC/PMMA ($\mu_p \approx 3800$ $cm^2V^{-1}s^{-1}$) scaffolds than the PC-only case ($\mu_p \approx 2500$ $cm^2V^{-1}s^{-1}$). These different trends can be explained by analyzing the extracted impurity carrier densities (n_0) in each case. Higher n_0 values translate to higher number of scattering impurities which can degrade the low-field mobility. For the PC case, the n_0 obtained is a factor of 1.5x greater (~0.27 $\times 10^{12}$ cm^{-2}) compared to all other cases (~0.18 $\times 10^{12}$ cm^{-2}); thus we expect slightly degraded mobility across graphene samples transferred using the PC scaffold as shown in Figure 4.7(c-d). This increase in n_0 is likely due to higher amounts of

polymer residues found on the surface of PC-transferred graphene samples, which is consistent with the higher h_{RMS} in Figure 4.1(e).

After the extended vacuum annealing, the reduction in *p*-type dopants previously observed (Figure 4.5) indicates that graphene E_F shifts closer to the conduction band. This effect is shown in Figure 4.8, where each averaged G band position is correlated to a measured E_F from Ref. [23]. This shift leads to an increase in hole R_C and a drastic reduction in electron R_C for all cases which went through the extended vacuum annealing, as seen in Figure 4.7(a-b). We note that in the case of the PMMA transfer annealed with the modified process (PMMA Mod.: green diamonds), the electron R_C reduction is not as pronounced compared to samples annealed with the extended process. Also hole *R*c degradation is more pronounced for the PMMA case compared to the PC, PC/PMMA or PMMA Mod. cases. This could be due to different graphene E_F shifts induced by each of the polymer scaffolds (i.e. PMMA, PC, etc.) and anneal conditions (mainly temperature and time). Additionally, strain could also contribute to a graphene E_F shift; thus, the electron and hole R_C and its variability vary amongst the three types of transferred graphene samples and the two types of annealing performed.

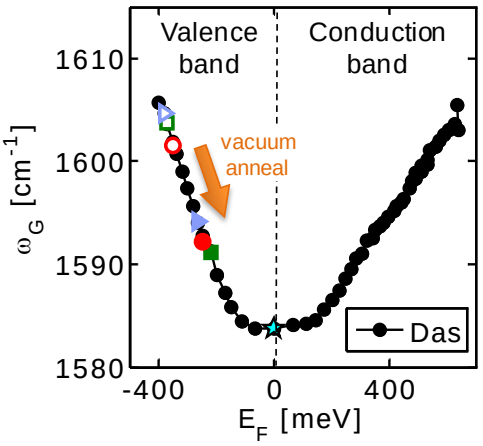

Figure 4.8. G band position (ω_G) as a function of measured E_F reproduced from Ref. [23]. Additionally, extrapolated E_F values for measured average G band positions (ω_G) from Fig. Figure 4.2 also included. Open (closed) symbols represent positions before (after) annealing, while PMMA, PC, and PC/PMMA based graphene transfers are represented by green squares, blue triangles, and red circles. Additionally, ω_G of exfoliated and suspended graphene (cyan star) yields $E_F \approx 0$ V indicating its intrinsic-like electronic behavior.

In the case of mobility after vacuum annealing, three other competing effects take place. First, graphene comes in closer contact with the SiO_2/Si substrate as previously reported [31]. As a result, graphene/SiO_2 interactions are enhanced, n_0 and impurity scattering increase (Table 4.1), and graphene mobility degrades proportionally [4]. Second, the annealing process helps to remove polymer residues from the graphene surface, resulting in a lower amount of surface scattering impurities and increased mobility, as shown for the PMMA Mod. case in Table 4.1. Third, the temperature and duration of this process can slightly damage graphene in the presence of oxygen molecules (even at low pressure) as observed by the ~0.2 to 0.4 average increase in the D-to-G integrated intensity ratio [Figure 4.3(e)] after the extended anneal. This increase is also consistent with an increased number of collisions (which could result in oxidation) between O_2 molecules with graphene in the extended vacuum anneal. We estimate that the total number of such "oxidizing/damaging" collisions for a 2-hour anneal at 200℃ (modified anneal) is ~900 per μm^2. While this result

may be considered negligible given the size of the O_2 molecule, that number goes up to ~30,000 per μm^2 for a 15-hour anneal at 300 ℃ (extended anneal). For details on how we arrived to this estimates please see Refs. [16, 32].

Table 4.1. Impurity carrier densities before and after vacuum annealing (V.A.) for each transferred case: PMMA, PC, PC/PMMA and PMMA Mod. The first three cases went through to the extended vacuum anneal, while the last one underwent the modified anneal. Average values are also provided to illustrate the overall increase of n_0 after the vacuum annealing process. *Values for PC before extended vacuum annealing (blue) and for PMMA Mod. after modified process (green) not included in average since they are statistically different from other cases.

Polymer Scaffold	n_0 [$10^{12}cm^{-2}$]	
	Before V.A.	After V.A.
PMMA	0.14 ± 0.03	0.58 ± 0.12
PC	0.27 ± 0.05*	0.60 ± 0.11
PC/PMMA	0.17 ± 0.03	0.49 ± 0.08
PMMA Mod.	0.22 ± 0.04	0.11 ± 0.01*
Average	0.18 ± 0.03	0.56 ± 0.10

4.6 Variability Analysis

We also quantify and analyze R_C and μ variability by comparing the standard deviations (*std*) and variation coefficients (c_v = *std*/*avg*) from each transferred case in Figure 4.9. In the case of R_C before vacuum annealing, the PC/PMMA transfer has a *std* for electrons (holes) 55% (30%) smaller than the PMMA case (Fig. S11). Additionally, c_v for electron R_C decreases by 9% while it remains nearly constant (< 1% decrease) for hole R_C (Figure 4.9). In the case of μ, once again the PC/PMMA bilayer results in decreased *std* (~56%) and c_v (~10%) for electrons, while in the case of holes we observe a degradation in *std* (~35%) and almost no change in c_v (~3%) respectively.

These dependencies demonstrate empirically that the PC/PMMA scaffold yields GFETs with reduced RC and μ variability, compared to those obtained from the common PMMA-supported graphene transfers. This effect is likely caused by the uniform surface in wrinkle-free graphene regions, negligible strain with a very small spatial variation (~0.00 ± 0.01 %), and a homogeneous doping level (relative to the other transferred samples) previously observed. Furthermore, we note that the exacted values for these R_C and μ variability parameters (i.e. *std*, c_v) may vary with a larger number of measured devices; however, based on consistent and repeatable AFM and Raman results we do not expect the relative variability trends to change drastically.

Ultimately, the annealing process conditions (i.e. temperature, time, pressure, etc.), the amount of surface polymer residues removed, and any potential anneal-induced graphene damage determine whether mobility improves or degrades. For our measured devices which underwent extended annealing (>10 hours), we observe a ~3x increase in impurity carrier density which leads to a factor of 2-3x degradation in mobility (Figure 4.7). However, a cooler and shorter modified vacuum anneal (T = 200 ^{o}C, t = 2 h, P = 10^{-5} Torr) induces less substrate impurities ($n_0 \approx 0.11 \times 10^{12}$ cm^{-2}) compared to the extended vacuum anneal ($n_0 \approx 0.58 \times 10^{12}$ cm^{-2}). As a result an increased mobility is observed in Figure 4.7(c-d) for the PMMA Mod. case in a similar manner than previously shown [4, 11, 21].

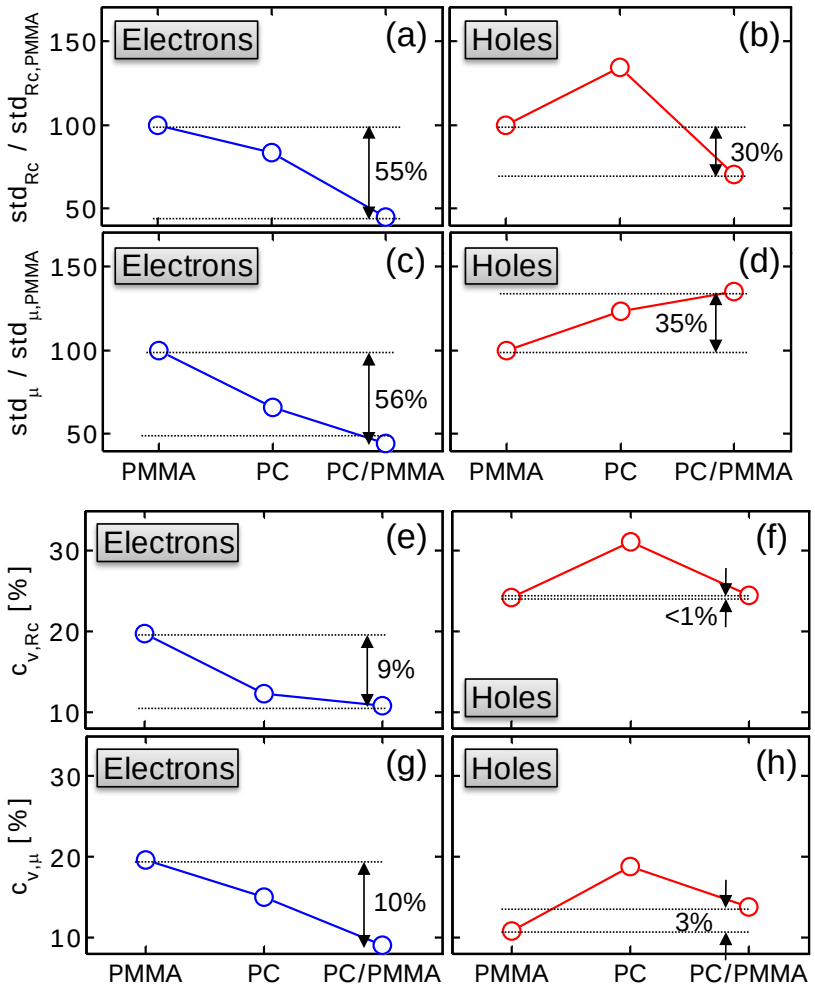

Figure 4.9. Electron (blue) and hole (red) contact resistance and mobility standard deviations (*std*) for all three transferred cases (PMMA, PC, PC/PMMA) normalized with the respective PMMA *std* before and coefficient of variation (c_v) for R_C and μ for each transferred case before (a-d).

4.7 Conclusions

In conclusion, we examined variability of surfaces, doping, strain, Raman signatures, contact resistance and mobility of GFETs from CVD-grown graphene, transferred with three different polymer scaffolds. These factors are affected differently by the amount of surface polymer residues present, and the mechanical and chemical interactions between graphene

and each polymer scaffold during transfer. We find that *before* vacuum annealing, the PC/PMMA scaffolds yield the smoothest surfaces in wrinkle-free regions, homogeneous doping concentrations, and negligible, spatially uniform strain. The combination of these factors is responsible for the improved device-to-device contact resistance and mobility variability. The PC/PMMA scaffolds should be particularly useful for transferring graphene onto substrates with low thermal budgets, such as plastics or similar fabrics. As diversification of graphene use and applications continue, understanding, minimizing, and quantifying device-to-device variability is expected to become ever more important for future practical applications, including circuit design.

4.8 References

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CHAPTER 5: SURFACE CHARGE DOPING OF GRAPHENE CONTACTS

In the previous two chapters we addressed graphene interface and quality issues by introducing a pulsed nanosecond characterization system (Chapter 3) and by optimizing the polymer-assisted transfer of graphene (Chapter 4). In this chapter, we address the issue of graphene contact resistance and its large variability. First, we explain in detail the origin of contact resistance, and how by increasing doping concentrations at the contact regions, we can decrease detrimental potential barriers and built-in potentials. Then, we characterize extensively the effect of doping on graphene at the contact regions via Raman and ultra-violet (UV) photo-spectroscopy techniques and electrical measurements. We find that the surface charge transfer between a graphene and Pd layer yields a Fermi level shift of ~0.2 eV which can be increased even further by doping graphene-under-metal with hydrochloric (HCl) and nitric acid (HNO_3) molecules. Finally, we discover that the doping of contact regions heavily influences the overall electrical characteristics of the channel and as a result electrical variability is improved drastically (from 30 to 80 %).

5.1 Contact Resistance Fundamentals

As we briefly mentioned during Chapter 2, contact resistance is one of the biggest issues currently limiting graphene nanoelectronics performance and development. However, this issue is not unique to graphene based electronics. In fact, contact resistance has also been a detrimental factor in Si [1-4] and III-V [5, 6] micro and nanoelectronics, becoming more

dominant as channel and contact dimensions have reached the nanometer scale [7, 8]. In these materials, in the absence of surface states, contact resistance is the product of a barrier height resultant from the difference between the metal work function and the semiconductor affinity (energy from vacuum level to top of conduction band). By doping the semiconductor material, this barrier can be made thinner such that thermionic emission, thermionic-field emission or field emission takes place. In the case of graphene contacts, the physical phenomena responsible for contact resistance are different. Overall, there are two main physical effects responsible for the high graphene-metal contact resistance as shown in the schematic in Figure 5.1(a): (1) carrier injection from the metal to the graphene underneath, and (2) transport of carrier from the graphene-under-metal to the gate-controlled channel.

In the case of the first process, metal-to-graphene carrier injection, we first consider the physical interactions at this interface. When the metal comes in contact with graphene a dipole forms at the interface with a finite metal-graphene physical separation d_{eq}, a built-in potential (ΔV) is created due to work function (Φ_M) differences [9], and the graphene Fermi level shifts (ΔE_{MF}) due to charge transfer with the metal [10]. These three interactions are shown in the band diagram of the metal-graphene interface in Figure 5.1(b). Furthermore, due to the graphene lower conductivity compared to metal contacts, current tends to crowd at the edges. This crowding generates a potential distribution along the edge of the contact over a given length, the transfer length (L_T, distance over which the V_{DS} generated potential drops to 1/e). Additionally, other effects such as the electronic coupling between metal, the cleanliness of the graphene-metal interface [11, 12] and the smaller graphene density of states (DOS) also contribute to increase contact resistance.

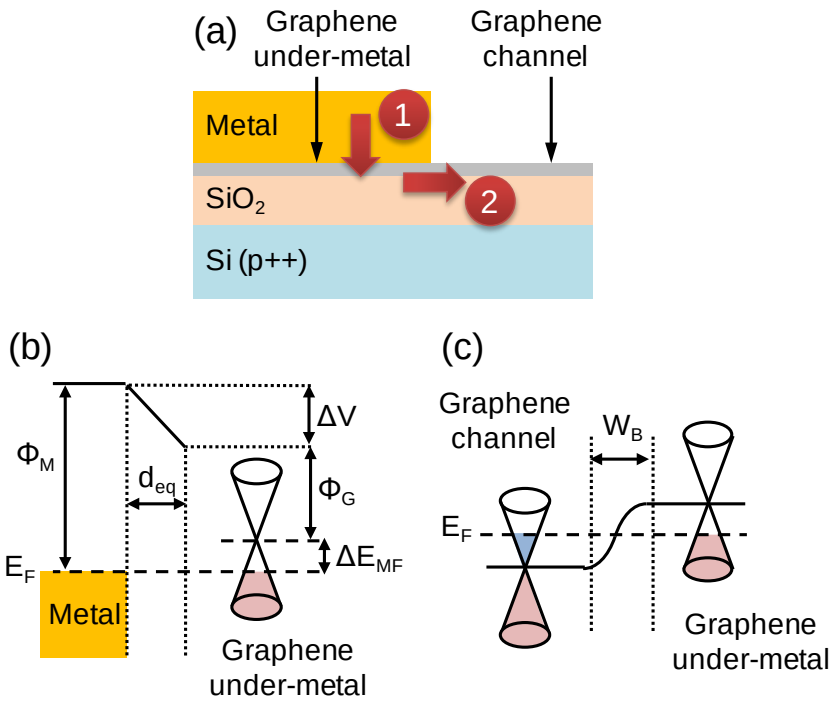

Figure 5.1. (a) Schematic of graphene contact and channel on a SiO_2/Si(p++) substrate. Sequential physical processes involved in the injection of carriers from carrier reservoir (metal) to channel: (1) metal to graphene-under-metal carrier injection and (2) transport to graphene channel. (b) Band diagram underneath graphene contact region and (c) between graphene underneath metal and graphene in channel. Note that panels (b) and (c) correspond to (1) and (2) shown in schematic from panel (a).

For the latter processes, carrier transport from the graphene-under-metal onto the gate-controlled channel, there are also detrimental physical interactions that result in increased contact resistance. As we mentioned earlier, metals tend to dope graphene via surface charge transfer [10, 13]. This modifies the graphene Fermi level and affects the sheet resistance and resistivity of the material under metal contacts. Thus the electrical characteristics of the graphene-under-metal and the gate-controlled channel are different. Ultimately this translates in the generation of a small built-in potential barrier [shown in Figure 5.1(c)] which extends into the channel and results in asymmetric electrical characteristics depending on biasing conditions. For example, if the metal shifts the graphene Fermi level at the contacts into its conduction band and the gate electrostatically moves the graphene Fermi level from the

channel into the valence band, a *p*-*n* junction forms at this interface. In this manner, depending on the channel biasing conditions and choice of metal, *p*-*p*′, *p*-*n*′, and *n*-*p*′ interfacial barriers can form. These barriers can in principle be very thin ($W_B \approx 20 - 100$ nm), but even then, they can significantly decrease the transmission probability of carrier injection from graphene-under-metal to the channel [9], thus increasing contact resistance. Furthermore, the creation of *p*-*n* junctions at the contact-channel interface leads to gate-voltage-dependent asymmetric electrical characteristics [14, 15].

Taking these two processes into account, in the following sections we heavily dope the graphene under the metal by a surface charge transfer method in order to (A) increase the number of available states (i.e. carrier density) facilitating metal-to-graphene charge injection and (B) decrease the built-in potential at the graphene-under-metal and graphene interface. Ultimately we hope these two outcomes help reduce contact resistance and enhance reproducibility and reliability amongst hundreds of devices measured.

5.2 Raman Spectroscopy and UV Photo-Spectroscopy

As we mentioned in the previous section, we want to heavily dope graphene under the metal contacts in order to help decrease contact resistance and device-to-device variability. However, the interaction between metals with graphene alone causes surface charge transfer which modifies the graphene Fermi level (E_F) even in the absence of a bias [13, 16]. This interaction has been demonstrated by using different metals [10, 17], thus introducing more available states that could participate in metal-to-graphene carrier injection and ultimately reduce contact resistance. By using this approach, Pd has been known to yield some of the lowest contact resistance values [9, 17] due to its high work function (~5.2 eV). On the other

hand, other works have indicated that the contact area between the grains of the metal and graphene [18] and the cleanliness of this interface [11, 19, 20] perhaps have a more dominant role than work function engineering alone. Furthermore, the contact resistance results obtained by work function engineering with different metals vary drastically from case to case. Therefore, in order to characterize thoroughly the surface charge doping in graphene with acidic *p*-type dopants, we need to take into account the changes induced by the metal.

We start by transferring CVD-grown graphene onto SiO_2(90 nm)/Si(p++) substrates using a PMMA polymer layer and wet-transfer process as described in Appendix A and similarly to our previous works [12, 21]. Then we anneal the samples for 2 h at 400 °C in a H_2/Ar flow in order to help remove polymer residues from the graphene surface. These residues have a detrimental effect on the metal-graphene interface, and minimizing their presence can decrease contact resistance [11, 19, 20] and reduce the variability from device to device [12]. Lastly we deposit a thin layer of Pd via electron-beam evaporation at a pressure of ~10^6 Torr.

Next we perform Raman spectroscopy measurement on each sample in order to determine and quantify the extent of the Pd influence in the graphene phonon vibrational modes. More details about the Raman spectroscopy technique used, such as laser power and energy and the fitting of the G and 2D bands can be found in Appendix B. Figure 5.2(a) shows typical graphene Raman spectra (normalized to the 2D peak intensity in each case) for bare graphene sample (green) and covered by a thin layer of Pd (gray). Schematics of each sample are shown in the inset. In both cases we can see that the 2D, G, and D peaks are present. By fitting a single Lorentzian function to the 2D and G peaks, we obtain 2D-to-G (I_{2D}/I_G) integrated intensities ratios which indicate monolayer graphene (4.5 ± 0.2 and 5.5 ±

0.5 for graphene-Pd and bare graphene respectively). Furthermore, we note that for the G band splits into two sub-bands G^+ and G^- component as shown in Figure 5.2(b) for graphene-Pd samples. This split has been previously reported for uniaxial anisotropic strain greater than ~0.4% [22] and for electronic interactions between metals (Ag, Ni and Ti) and graphene [23, 24]. In both of these cases, the degeneracy between inter-valley transverse (iTO) and longitudinal (LO) optical phonon modes near the Γ point is removed, leading to the aforementioned G band split.

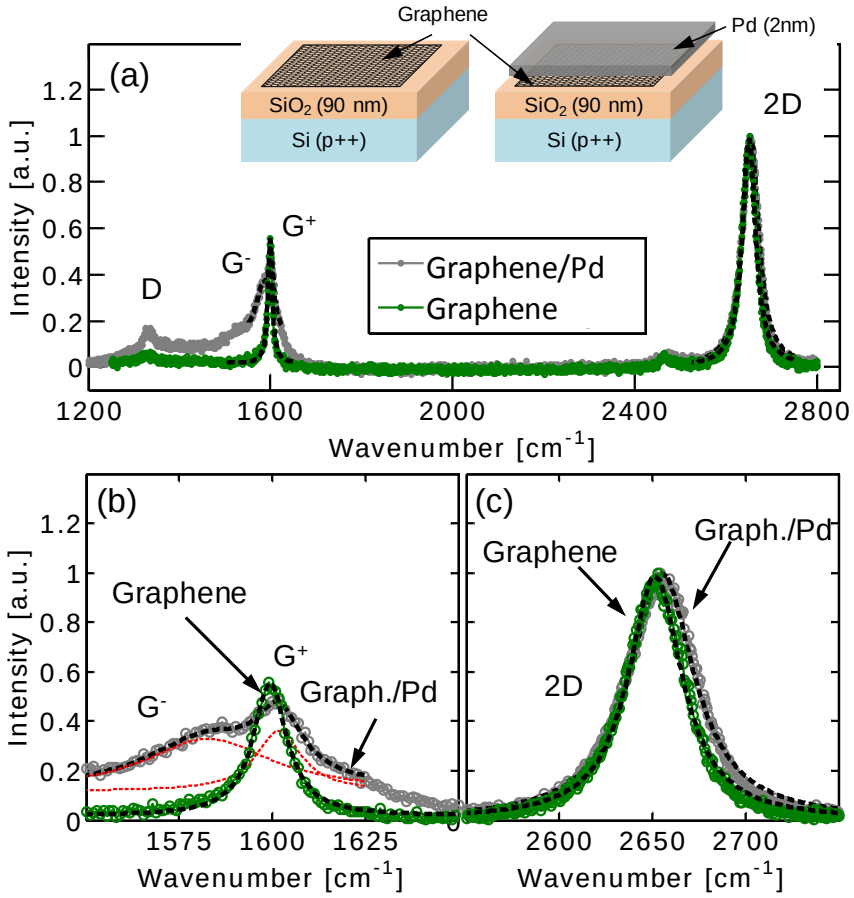

Figure 5.2. (a) Raman spectra of bare graphene (green) and graphene covered by 2nm of evaporated Pd (gray). Inset shows schematic for each case (bare graphene and covered with Pd) on a SiO_2(90 nm)/Si substrate. Zoomed in regions corresponding to the (b) G and (c) 2D bands are also shown. Note that the Raman spectrum from the graphene-Pd sample, results in slight splitting of the G band into G^- and G^+.

Since we do not anticipate the presence of excessive strain in our samples even in the presence of a thin Pd layer, we believe that the splitting observed is related to the Pd-graphene electronic interactions. Finally, we observe that both the G^+ sub-band and the 2D band slightly blue-shift after deposition of Pd. These two factors (G band splitting and blue shift of 2D and G bands) indicate that the electronic structure of graphene is heavily affected by its interaction with Pd.

Now that we have a reference of graphene Raman spectra affected by the metal-contact interactions, we examine samples in which the graphene surface is doped *p*-type before deposition of the Pd layer (also 2 nm). To achieve this, we use two types of *p*-type dopants molecules in solution, also known to effectively donate holes to carbon nanotubes [25] and graphene [26, 27]: hydrochloric (HCl) and nitric acid (HNO_3). Each graphene sample is immersed in a 63 wt% and 36 wt% diluted solutions (1:1 with H_2O) of HNO_3 and HCl respectively for 1, 10 and 100s. In this manner we hope to control the amount of doping that can take place in each case. Modifying the concentration of each acid was also a possibility, but these concentrations were chosen based on compatibility with our lithography processes. The exposure of graphene to these acids leads to air-stable surface charge transfer resulting in a Fermi level shift, an increased carrier concentration and a decrease in sheet resistivity. Finally, we note that the ensuing Pd layer was deposited for all samples during the same evaporation, thus maintaining evaporation conditions (and metal granular composition) the same.

In Figure 5.3 we observe the positions of the 2D band and G^+ and G^- sub-bands for the bare undoped graphene (green lines), the undoped graphene-Pd (from Figure 5.2), and the HCl (red diamonds) and HNO_3 (blue circles) doped graphene-Pd cases as a function of

doping time before and after an optimized vacuum annealing process. Each point in Figure 5.3 represents an average peak position obtained from over 150 spectra measured for each condition and fitted with a Lorentzian peak (as shown in Figure 5.2); the error bars in each case correspond to one standard deviation. Before the vacuum anneal [Figure 5.3(a)] we note a similar splitting of the G band in the doped graphene-Pd samples, indicating that Pd still affects the graphene Fermi level and thus doping concentration. Furthermore, we note that the G^+ sub-band red shifts when doped with either HCl or HNO_3 compared to graphene-Pd samples, while the G^- sub-band remains fairly constant (within the margin of error) regardless doping duration and acid type. This shift in peak positions in the doped graphene-Pd samples compared to the undoped graphene-Pd (gray line) indicates that the acid treatment has successfully modified the graphene Fermi level. Additionally we see that as doping duration is increased to 10 s the G^+ peak position of the HNO_3 graphene-Pd sample is blue shifted. This time dependent shift of the G^+ sub-band suggests that the graphene-HNO_3 reaction might be more time sensitive than the one with HCl. In the case of the 2D peak position [Figure 5.3(c)] it is difficult to differentiate a single trend as doping time is increased for either acid. We note that for both cases and doping durations the 2D peak is blue shifted with respect to the bare undoped graphene sample (green line); however, this is not the case with respect to the 2D peak position of the graphene-Pd sample.

Additionally, since we typically anneal graphene FETs in order to improve the contacts and electrical characteristic, we also recorded all peak positions after an optimized 2 h vacuum anneal at 200 °C (similar to that one in Chapter 4). The results are shown in Figure 5.3(b) and (d). Overall we observe a red shift on the G^+ sub-band for all samples (doped or undoped or bared or covered by Pd) while the G^- sub-band and 2D bands do not change

drastically. This behavior has been previously observed in Chapter 4 and in other works [28, 29] and it is evidence of a Fermi level shift towards the graphene conduction band, resulting in a decrease of *p*-type dopants [12]. We note that all these shifts in the 2D and G bands could be related to changes in the Fermi level and hence doping, as well as the presence of compressive or tensile strain. In Chapter 4 we adapted a Raman vector model [30] in order to separate their individual contributions. However, although using that model could be an option here, we perform UV photo-spectroscopy measurements to direct determine changes in the Fermi level and more accurately calculate the respective carrier concentrations achieved with doping.

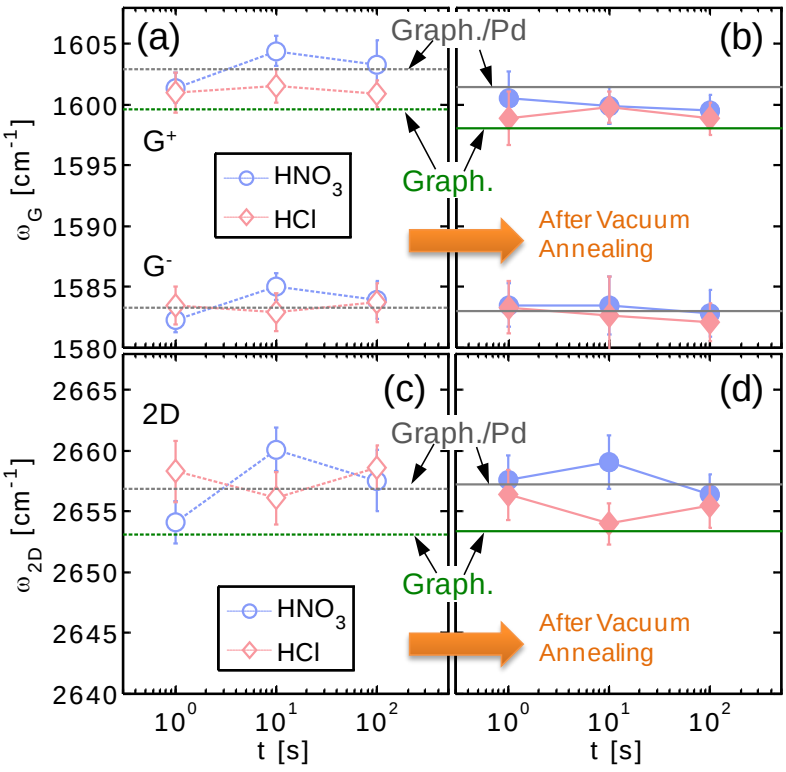

Figure 5.3. (a-b) Average G band and (c-d) 2D band peak positions before (open symbols and dashed lines) and after (closed symbols and solid lines) vacuum annealing for undoped bare graphene (green lines), undoped graphene-Pd (gray lines), HCl doped graphene-Pd (red diamonds) and HNO_3 doped graphene-Pd (blue circles) as a function of doping time (1, 10, 100 s). Error bars in each case denote one standard deviation obtained from over 150 spectra collected for each sample.

Figure 5.4(a) and (b) show the measured graphene work function (Φ) before and after vacuum annealing respectively. We note that before vacuum annealing, the work function of undoped graphene-Pd ($\Phi_{\text{graphene-Pd}}$) increases by ~0.27 eV compared to the bare pristine graphene sample (Φ_{graphene}). This indicates that the Fermi level shifts further into the valence band due to charge transfer interactions with the metal, such that: $\Delta E_F = \Phi_{\text{graphene-Pd}} - \Phi_{\text{graphene}}$. Similarly, we observe that HCl and HNO_3 chemical treatments increase the graphene-Pd work function even further for all doping durations. In the case of HCl, the calculated Fermi level shift is between 0.38 and 0.41 eV and is fairly constant for doping durations from 1 to 100 s, while for HNO_3, the increase ranges from 0.39 to 0.59 eV for longer doping times. This latter behavior has been previously measured in bare graphene samples doped with HNO_3 [26, 27], and could be attributed to a slower transfer of charge taking place at the graphene surface. After the vacuum annealing process, the work function for all samples decreases, indicating a Fermi level shift towards the graphene conduction band and reduction in hole doping density. We note that all of these work function measurements are done through a thin layer of Pd, which could introduce certain anomalies in actual numbers obtained.

Finally, from the differences in Fermi level (ΔE_F) we can calculate the respective carrier concentrations. We do this by integrating the graphene density of states and the Fermi-Dirac distribution over all possible energies as shown in Eq. 5.1 and in Ref. [31]. The solution of this expression is given by Eq. 5.2, where k is the Boltzmann constant, T the temperature, v_F the Fermi velocity (~10^8 cm/s), $\hbar$ the reduced Plank's constant, $\Im(\eta)$ is the Fermi integral and $\eta = \Delta E_F / kT$. Using the Fermi level differences calculated from Figure 5.4, we obtain hole density increases of ~11×10^{12} cm^{-2} and up to ~27×10^{12} cm^{-2} for the HCl and

HNO_3 doped graphene-Pd cases respectively. We also see that the metal alone is responsible for increasing hole carrier concentration by ~5.8×10^{12} cm^{-2} due to graphene-metal interface interactions. Finally we note that after vacuum annealing, the increase in hole carrier concentration for each case decrease drastically ($\Delta p \approx 11 \times 10^{12}$ cm^{-2}).

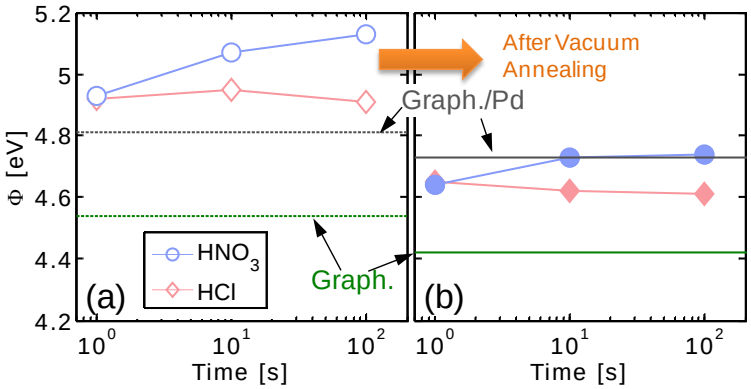

Figure 5.4. Graphene work function (Φ) measured by ultra-violet (UV) spectroscopy (a) before (open symbols) and (b) after (closed symbols) a 2 h at 200 °C vacuum annealing process for undoped bare graphene (green lines), undoped graphene-Pd (gray lines) and HCl (red diamonds) and HNO_3 (blue circles) doped graphene-Pd samples as a function of doping time (1, 10, 100 s).

$$n = \int_0^\infty dE \rho_{gr}(E) f(E) \qquad \text{Eq. 5.1}$$

$$\Delta n = \frac{2}{\pi}\left(\frac{kT}{\hbar v_F}\right)^2 \Im(+\eta = \Delta E_F / kT) \qquad \text{Eq. 5.2}$$

5.3 Electrical Characterization

In this section we incorporate the previously characterized doped-graphene sheets into the channel and the contact regions of graphene field-effect transistors (GFETs). With these implementations we measure doped graphene sheet resistance, its temperature stability and

the effect it can when placed in the contact regions of GFETs. First, we fabricate graphene FETs on SiO_2(90 nm)/Si(p++) substrates with Pd (40 nm) as the contact metal contact as outlined in Appendix A and in a similar manner than in our previous works [12, 21]. The channel length (L) and width (W) range from 2 to 10 μm. Next, we immerse each chip in similar concentrations of HCl and HNO_3 solutions for 1s. In this manner we dope the unexposed graphene channels and measure their electrical characteristics.

Figure 5.5 shows the resistance (R) vs. gate voltage (V_G) characteristics measured in vacuum ($P = 10^{-5}$ Torr) before and after doping at room temperature (25 °C) and up to 200 °C. First of all, we note that at room temperature the Dirac voltage significantly shifts (ΔV_0) towards gate voltages higher than ~40V for both cases (HCl or HNO_3). In the case of HCl doped GFETs $\Delta V_0 \approx 60$ V which translates to a hole density increase of $\sim 14 \times 10^{12}$ cm^{-2}, while for HNO_3 doped FETs ΔV_0 is outside of the applied V_G range (-40 to 40 V). Additionally, we note that resistance decreases by factors of ~10 and 35x respectively near the Dirac point of the original undoped FET (R_{max}) compared to the doped cases (R_{V0}). This drastic decrease in resistance is further proof that hole carrier densities drastically increased and the Fermi level has been shifted. However, as we increase the temperature up to 200 °C, V_0 of the HCl doped GFET shifts back towards its original undoped position and correspondingly sheet resistance increases. In the case of HNO_3 doped GFETs, the sheet resistance also increases with increasing temperature and the point of minimum conductivity starts to become visible within the tested range of gate voltages; however, the previously undoped transfer characteristics (gray squares in [Figure 5.5(b)]) are not fully recovered. These temperature instabilities in the transfer characteristics of uncovered GFETs doped with either acid indicate that the extra surface charge responsible for doping can be removed as

temperature increases. This issue could potentially pose a major reliability problem since graphene devices are known to exhibit significant self-heating effects [21, 32, 33] when operating at relatively high lateral (>1 V/μm) and transverse fields (>1 MV/cm). Furthermore, we note that surface charge might behave differently while covered by the metal contacts; however, more extensive temperature dependent sheet resistance measurements of graphene-metal samples are needed in order to properly characterize these effects.

Next, in Figure 5.6 we compare the average resistance ratio (R_{max}/R_{V0}) and sheet resistance ($R_{sh} = R \times W/L$) values for HCl and HNO_3 doped GFETs; each point corresponds to the average of 5 different devices while the error bars represent one standard deviation. Once again, we observe trends similar to those observed in the gate voltage dependent data: the progressive increase in sheet resistance as temperature increases, and the decrease in the resistance ratio measured at the Dirac point of the original undoped device.

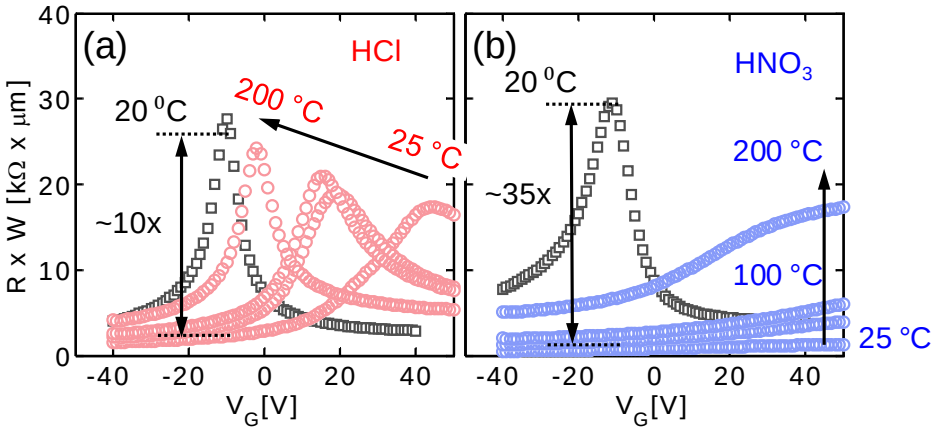

Figure 5.5. (a) Resistance (R) vs. gate voltage (V_G) electrical for undoped channel of graphene FETs (gray squares) and HCl (red) and (b) HNO_3 (blue) doped graphene channels for temperatures ranging from 20 to 200 °C. Doping in each sample was done for 1 s. Note that the ratio between resistance at Dirac point of undoped sample $R_{max} = R(V_G = V_0)$ and resistance after doping at same V_G is around 10 and 35 for HCl and HNO_3 doped samples respectively.

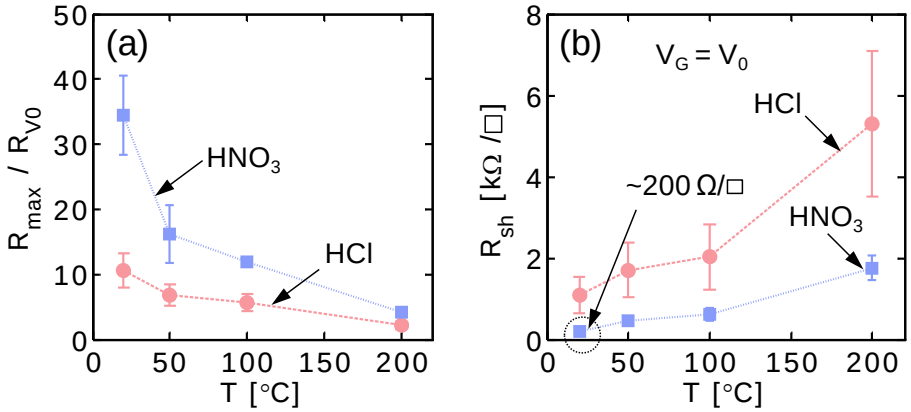

Figure 5.6. (a) Ratio between resistance at Dirac point of undoped samples (R_{max}) and HCl and HNO_3 doped samples at the same gate voltage (R_{V0}) as a function of temperature. (b) Sheet resistance (R_{sh}) as a function of temperature for each doped samples. Error bars correspond to one standard deviation amongst 5 samples measured at each temperature.

Up to this point we have found that via charge transfer doping with the mentioned acids (HCl and HNO_3) the graphene Fermi level shifts deeper into the graphene valence band. This Fermi level shift (ΔE_F) affects the 2D and G Raman peak positions, increases the carrier concentration (up to ~27×10^{12} cm^{-2} for the HNO3 case) and decreases sheet resistance (down to ~200 Ω/□). Next, we attempt to use this low resistivity material at the contact regions (under Pd contacts) in order to improve contact resistance and device-to-device variability.

The fabrication of this set of GFETs is similar to the one described in our previous works [12, 21] and earlier in this chapter. The contact regions are defined with photo-resist (PR) and UV-lithography. After PR exposure and development the graphene contact regions remain exposed to air while the graphene channel remains protected from the environment. At this stage, the chips are immersed in diluted solutions of HCl and HNO_3 for ~180 s. This doping duration is the longest time for which the given acid concentrations do not attack the developed PR patterns. Finally, after exposure to the dopants in solution, 40 nm of Pd are deposited by electron-beam evaporation. We note that doping the graphene-under-metal is

the last step of our fabrication process, thus ensuring that other processing related factors (such as bakes and anneals) do not affect the underlying doped graphene.

Figure 5.7 shows results of the electrical characteristics measured in vacuum of undoped (gray), HCl (red) and HNO_3 (blue) doped contacts for over 180 GFETs before and after a 2-h 200 °C vacuum annealing process. We note that in all cases there is a certain level of variability in the position of the Dirac voltage (~10 to 15 V), the saturated resistance (indicative of contact resistance) and the width near the Dirac point (indicative of mobility). More specifically, before vacuum annealing, the saturated resistance is visibly lower for the HCl and HNO_3 doped contact cases [Figure 5.7(b) and (c)] compared with the undoped case [Figure 5.7(a)]. Even more, after vacuum annealing, the saturated resistance and Dirac voltage of the HCl doped contact case become drastically more uniform. Ultimately, all of these factors indicate that the doping treatment has successfully decreased contact resistance, and in combination with the annealing process, it has helped to drastically reduce variability.

Next, we examine contact resistance for each case and their variations more rigorously. For this purpose, we extract contact resistance (R_C) using a transport model described previously [33, 34] and used in Chapters 3 and 4. The results of this extraction are shown in Figure 5.8. Before vacuum annealing (open symbols) electron R_C is ~11 and 32% smaller for GFETs with HCl and HNO_3 doped contact respectively when compared to GFETs with undoped contacts. In a similar manner, for hole transport the decrease in R_C is not as evident for the HCl doping of contacts (~7%) while it is clearly marked for the HNO_3 doping (43%). The lowest R_C value obtained correspond to those of GFET with HNO_3 doped contacts (electron $R_C = 2.80 \pm 0.62$ kΩ·μm, hole $R_C = 1.43 \pm 0.42$ kΩ·μm). We note that these R_C

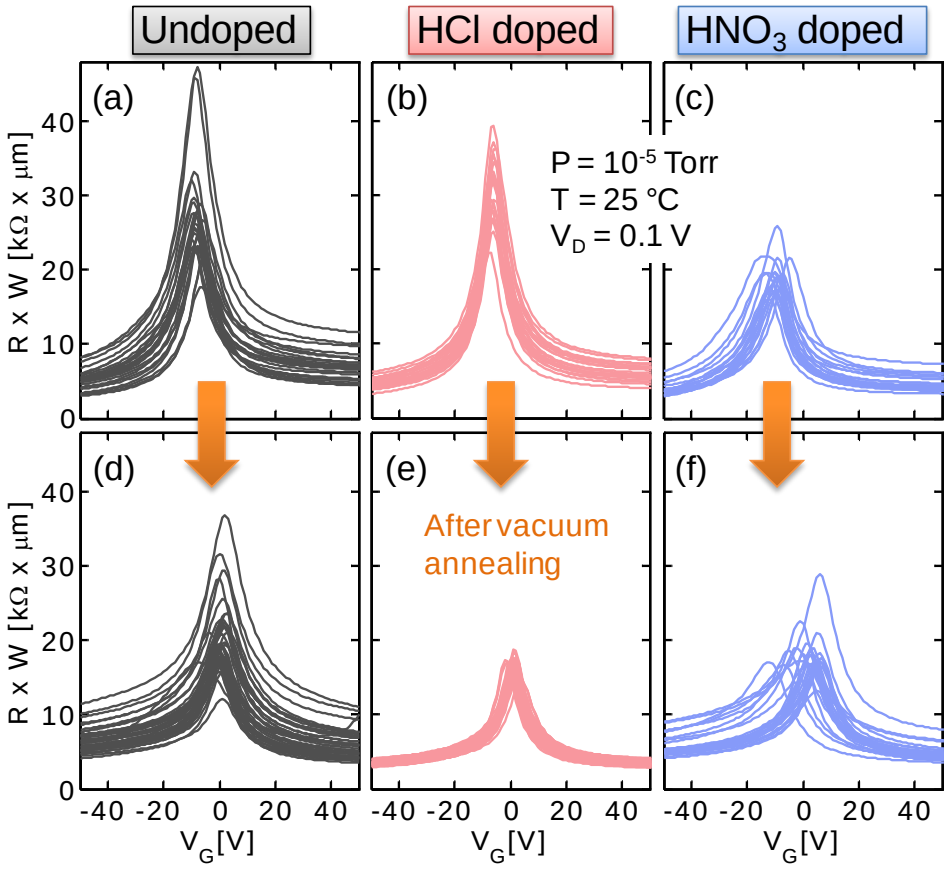

Figure 5.7. Graphene FET resistance (R) vs. gate voltage (V_G) characteristics with undoped (gray), HCl (red) and HNO_3 (blue) doped graphene contacts (a-c) before and (d-f) after a 2 h 200 °C vacuum annealing process. All measurements done in vacuum (P = 10^{-5} Torr) and at room temperature (T = 25 °C). Device channel lengths (L) and widths (W) range from 2 – 10 μm.

values, are not lower than many previously reported works or even than those found in Chapter 4; this is due to the lower quality of this particular graphene growth (compared to those in Chapter 4). However, the relative R_C decrease with chemically treated contacts remains an encouraging improvement. These marked electron and hole R_C reductions in a large number of measured GFETs indicate improvements of different mechanisms in each case. In the case of hole R_C, sheet resistance at the contacts decreases and transport into the channel becomes less resistive by increasing the graphene-under-metal hole carrier concentration. Furthermore, a higher number of available conduction modes are always

present in the graphene-under-metal compared to those in the channel region [9]. In the case of electron transport, we hypothesize that the metal-graphene interface becomes cleaner after chemical treatment with acids, since based on the work function increase (Figure 5.4) we expect electron concentration to decrease (and R_C to increase). However, AFM or cross-sectional SEM characterization of this interface is necessary in order to confirm the validity of this claim. We note that several studies have shown R_C and variability reductions [11, 12, 19, 20] by improving the cleanliness of the metal-graphene interface.

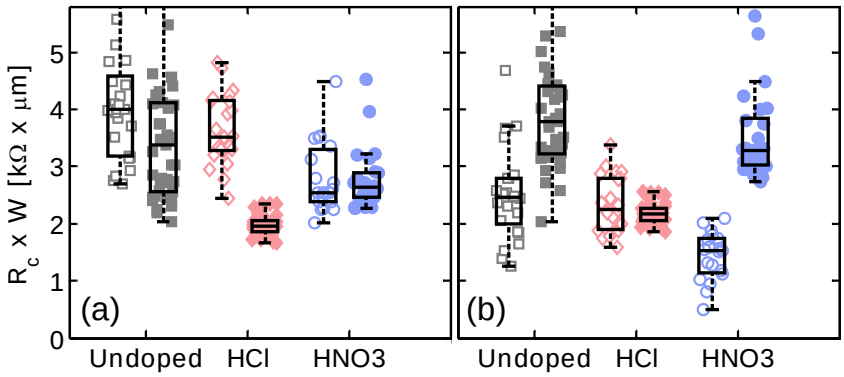

Figure 5.8. (a) Electron and (b) hole contact resistances extracted from fitting of transport model for undoped (gray squares), HCl (red circles) and HNO_3 (blue circles) doped contacts of graphene FETs before (open symbols) and after (solid symbols) an optimized vacuum annealing process ($P = 10^{-5}$ Torr, $t = 2$ h, $T = 200$ °C). Contact resistance vales shown are extracted at carrier density equal to 5×10^{12} cm^{-2}.

After vacuum annealing (closed symbols), the graphene-Pd work function decreases for both the HCl and HNO_3 doped samples, as shown in Figure 5.4(b); therefore we expect hole R_C to increase and electron R_C to decrease for all cases (undoped and doped). However, while in the undoped and HNO_3 doped contacts cases (gray and blue solid symbols) R_C follows these behaviors, in the HCl doped contact case (red solid circles) it does not. Here, we observe that hole R_C remains fairly constant (<6 % change) after the vacuum annealing, while electron R_C decreases by 43%, the standard deviation amongst measured devices (*std*)

decreases ~80% and a the normalized standard deviation ($c_v = std/R_{C\text{-}avg}$) decreases by ~70% (compared to the undoped contact sample). These statistics suggest that other effects such as graphene-metal interface cleanliness and enhanced metal-graphene electronic coupling become more important for the reduction of R_C and its variability than Fermi level positions and carrier concentrations alone. This has been previously suggested for metal based doping of graphene [14] and it also seems to be the case for the acid doped graphene contacts studied here. Finally, we note that while the reported work function increase for the doped graphene-Pd samples (Figure 5.4) is beneficial to increase hole carrier concentration, it could also potentially increase the built-in potential barrier (W_B) between the graphene-under-metal and gate-controlled channel (Figure 5.1). However, we do not measure asymmetries in the electrical characteristics typical of these situations [35-38].

5.4 Conclusions

In conclusion, in this chapter we have shown that via surface charge transfer doping with nitric and hydrochloric acids, the graphene Fermi level can be modified and induce *p*-type doping. We measured the resultant changes in bare graphene and Pd-covered graphene samples by using Raman and ultra-violet photo spectroscopy. These material characterization techniques allow us to directly measure the Fermi level shift in the graphene underneath Pd contacts and calculate changes in hole carrier concentration. Furthermore, by exposing bare graphene and graphene-under-metal contacts to these dopants, we decrease sheet and contact resistances respectively. Finally we show a significant decrease in contact resistance variability of samples whose contact regions were treated with HCl, suggesting that the cleaning of the metal-graphene interface is as important, if not more, as simply doping of

graphene alone. All of these findings will be important when considering new research directions in order to satisfactorily overcome the hurdle of contact resistance.

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CHAPTER 6: CONCLUSIONS AND FUTURE WORK

6.1 Conclusions

In summary, in this dissertation we have shown experimental work towards the development of higher performing graphene based nanoelectronics. Throughout this study we fabricated large-scale CVD-grown graphene and characterized its material and electrical properties using a wide array of techniques. We used a field-effect-transistor configuration since it allowed us to modulate graphene carrier concentrations while dealing with three of the most prominent issues in the field of graphene electronics: interfaces, material quality and contacts. Throughout this dissertation we have addressed each one of those issues.

First, we developed a nanosecond pulsed measurement technique which allowed for the reliable characterization of graphene field-effect transistors (GFETs) despite the presence of "imperfect" interfaces. With this measurement technique, we characterized charge interface and bulk trapping time constants, and managed to circumvent some of the detrimental factors which negatively affect transport. We were able to eliminate Dirac voltage instabilities (analogous to threshold voltage instabilities in Si CMOS) and ultimately extract parameters of interest such as transconductance and mobility reliably. We also briefly studied the effects of charge trapping at high lateral fields, and showed that by limiting the amount over which carrier can become trapped, trapping decreases. Additionally, our pulsed measurement technique can be extended to study other material interfaces and investigate trapping time constants present in several semiconductor/oxide interfaces.

Next, we investigated variability of graphene transistors from large-scale growth by chemical vapor deposition after transfer to SiO_2/Si substrates using three different polymer scaffolds. We quantified mobility, contact resistance and residual impurity variability by electrical measurements, as well as strain and doping spatial homogeneities by extensive Raman analysis and atomic force microscopy. We found that depending on thickness and composition, each scaffold induces different graphene-polymer mechanical and chemical interactions during transfer, resulting in changes of surface roughness, doping and strain. Additionally, we found that electrical variability, doping, and strain are minimized with a bilayer polycarbonate (PC) and poly(methyl methacrylate) (PMMA) scaffold used to transfer graphene. This study provides a better understanding of variability in graphene devices, and paves the way to more reliable and repeatable graphene circuits.

Finally, we decreased the contact resistance and variability of graphene FETs via surface charge transfer with acidic molecules in solution. We thoroughly characterized the effect of the doped graphene and its effects in Raman and UV-photo spectroscopy measurements. From these measurements, we were able to calculate shifts in Fermi level and carrier concentration. Lastly, we showed that the electrical characteristics of *p*-type doped graphene channels can drastically decrease sheet resistance. Furthermore, by applying these same doping techniques to the graphene contact regions, we decreased contact resistance and drastically reduce electrical variability.

The work presented in this dissertation presents a thorough foundation of the main experimental hurdles in the development of graphene nanoelectronics and viable approaches to overcome them. Ultimately the large-scale industrial implementation of graphene depends

on our ability as a scientific community to overcome these obstacles and obtain intrinsic-like graphene potential in an efficient, reliable and cost effective manner.

6.2 Future Work

As we have discussed and shown throughout this work, graphene exhibits great potential in a wide range of areas due to its unique and exciting physical properties. However, the future of graphene based nanoelectronics will depend on the ability to overcome developmental hurdles and achieve process integration and large-scale cost-effective implementations.

More specifically, decreasing contact resistance is one of these major obstacles, since it limits device characteristics and degrades performance. Recently, edge-injection contacts have shown great promise towards resolving this issue; however, the ideal graphene-to-metal contact will require even more enhanced electrical interaction via covalent bonding.

In the case of research in graphene interfaces and material quality, the past few years have been exciting. The demonstration of pristine clean charge-free graphene-hexagonal-boron-nitride (hBN) interfaces and the wafer-scale grain-boundary-free growth of graphene on semiconducting substrates like Ge show great promise. However, the key factor for future works in these areas of research will be the successful large-scale implementation and consecutive controlled growth of graphene-hBN heterojunctions. These kinds of chemically controlled architectures could provide easily accessible and reliable graphene electrical characteristics unaffected by the environment. Additionally, hexagonal boron nitride could be used as an isolation layer material between graphene and other interfaces, thus preventing major detrimental effects.

APPENDIX A: GRAPHENE GROWTH AND TRANSFER

Cu foil pre-treatment: Graphene is grown on a Cu substrate (Alfa Aesar, 0.025 mm thick, 99.8%) treated in a dilute 2:1 de-ionized H_2O to hydrochloric acid (HCl) solution (fw. 36.46) for 3 minutes. This cleans and partially etches a thin layer from the Cu surface.

Graphene growth: Growth takes place in a 1-inch CVD furnace. First, the Cu foil is annealed for 1 h at 1000 °C in order to increase Cu grain size under a H_2/Ar flow at ~1 Torr. Next, methane is introduced for 20 to 25 min. Finally, the furnace is cooled down to room temperature under methane flow for ~1 to 2 h. Graphene growth is confirmed on both surfaces (i.e. top and bottom) of the Cu foil with Raman spectroscopy.

Graphene transfer: First we deposit the different polymer stacks used in this study on one of the surfaces of the graphene/Cu/graphene samples. For the PMMA case, we use two PMMA layers (495K A2 and 950K A4) in order to end up with a final scaffold of ~300nm. Each PMMA layer is spun at 3000 rpm for 30 s and baked at 200 °C for 2 min. For the PC case, a 1.5 wt% by volume solution of PC dispersed in chloroform is spun at 3000 rpm for 30 s. For the PC/PMMA case, we first spin a PC layer at 5000 rpm for 30 s; this spin rate is chosen such that after adding one extra layer of PMMA (950K A4 at 3000 rpm for 30 s) the final thickness of the PC/PMMA scaffold is comparable to the PMMA only cases. The final thickness of each polymer scaffolds is determined by profilometry: PMMA ≈ 290 nm ± 10 nm, PC ≈ 70 nm ± 20 nm and PC/PMMA ≈ 295 nm ± 10 nm.

Next, graphene is etched from the unprotected polymer-free graphene/Cu/graphene surface by O_2 plasma (~80 W for 30 s). Then the Cu foil is etched overnight in a $FeCl_3$ solution. This process results in a graphene/polymer-scaffold stack floating on the surface of the etchant solution. Subsequently, this stack is transferred with a clean glass slide to three successive 15 min. baths (DI H_2O, 2:1 DI H_2O:HCl, and DI H_2O) to clean and remove residues from the Cu etching process. Finally, the graphene/polymer-scaffold stack is removed from the last DI H_2O bath using a highly doped p++ Si substrate (ρ = 0.005 Ω·cm) with a thermally grown SiO_2 (90 nm) layer on top.

Graphene drying and polymer scaffold lift-off: In order to lift off the polymer scaffolds while minimizing graphene damage (i.e. holes or large tears) it is important to remove water from the SiO_2/graphene interface and the graphene/polymer surface. For this reason samples are left to dry in air for 2 to 3 h followed by a soft bake on a hot plate (50 °C for 5 min and ramp to 150 °C for 15 min) as done in Ref. [1]. We note that the exact temperatures and durations of this soft bake may not be critical for a successful transfer; however, it is important to heat up samples past 100 °C at least since it partially removes water from the SiO_2/graphene interface and it facilitates lift-off.

Next we proceed to remove the respective polymer scaffolds from the graphene surfaces. For the PMMA case we use a 1:1 dichloromethane and methanol solution for 40 – 60 min. followed by simple degreasing with acetone, methanol, and isopropanol. For the PC and PC/PMMA cases we use three different baths followed by similar degreasing. First we use a 1:1 mixture of chloroform and acetone, followed by just chloroform, and finally just acetone. Samples are left inside each bath for ~15 min. Finally, we anneal all samples in equal parts flow of H_2/Ar at 400℃ for 2 h.

A.1 Reference

[1] X. Liang, B. A. Sperling, I. Calizo, G. Cheng, C. A. Hacker, Q. Zhang, Y. Obeng, K. Yan, H. Peng, Q. Li, X. Zhu, H. Yuan, A. R. Hight Walker, Z. Liu, L.-m. Peng, and C. A. Richter, "Toward Clean and Crackless Transfer of Graphene," *ACS Nano,* vol. 5, pp. 9144-9153, 2011.

APPENDIX B: RAMAN SPECTROSCOPY AND ANALYSIS

Raman spectroscopy is done using a Renishaw Raman spectrometer with a 633 nm excitation laser. The laser power and spot size diameter are ~1.3 mW and ~1.2 μm respectively. Additionally, we fit the 2D and G bands using a Lorentzian of the form:

$$L(\omega) = \frac{2A}{\pi} \times \frac{F}{4 \cdot (\omega - \omega_{2D/G})^2 + F^2} + B \qquad \text{Eq. B.1}$$

where ω is wave number, $\omega_{2D/G}$ corresponds to the 2D or G band peak positions, A is the area under the Lorentzian curve, F is the full-width-at-half-maximum (FWHM) and B is the baseline used as offset. An example of such fitting (red dashed lines) is shown in Figure B.1 for CVD-grown and H_2/Ar annealed graphene supported on SiO_2 (black circles) and non-annealed suspended exfoliated graphene (blue squares) similar to that used in Ref. [1]. Fitting parameters (peak positions, FWHM and area ratios) from this fitting process are summarized and analyzed in Chapters 4 and 5.

Furthermore, the presence of a small and broad D peak and a broad G peak in the H_2/Ar annealed CVD graphene from Figure B.1 indicates that hydrocarbons could be present on the surface [2] and/or that Raman-active defects have been introduced by the anneal. Table B.1 shows the average peak positions for the 2D and G bands for the three transferred cases described in Chapter 4, before and after a vacuum annealing process.

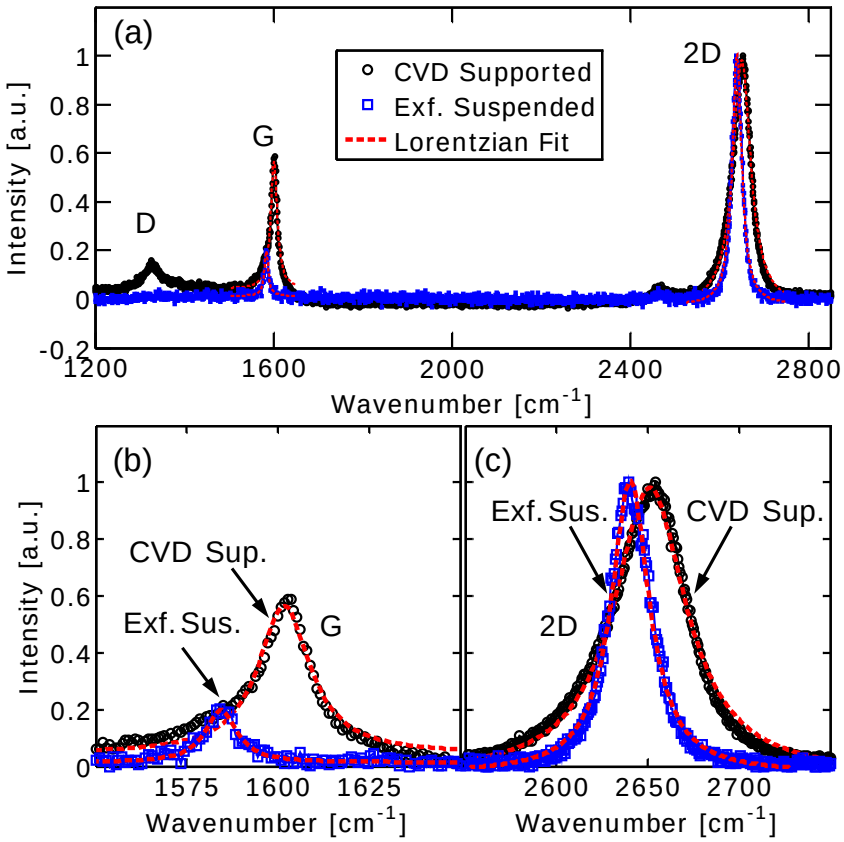

Figure B.1. (a) Measured Raman spectra of CVD-grown graphene on SiO_2 (black circles) and suspended exfoliated graphene (blue squares) with Lorentzian fits (red dashed lines) of G and 2D bands. Close up of (b) G and (c) 2D bands from panel (a).

Table B.1. Peak positions for 2D and G bands for all graphene transferred cases before and after vacuum annealing (V.A.).

Polymer Scaffold	ω_{2D} [cm^{-1}]		ω_G [cm^{-1}]	
	Before V.A.	After V.A.	Before V.A.	After V.A.
PMMA	2652.5 ± 1.3	2649.4 ± 2.0	1603.7 ± 0.8	1591.2 ± 1.7
PC	2657.4 ± 1.6	2655.9 ± 0.7	1604.7 ± 0.7	1594.7 ± 0.5
PC/PMMA	2651.8 ± 1.4	2652.5 ± 1.2	1601.6 ± 0.8	1592.2 ± 0.9

B.1 References

[1] V. E. Dorgan, A. Behnam, H. J. Conley, K. I. Bolotin, and E. Pop, "High-Field Electrical and Thermal Transport in Suspended Graphene," *Nano Letters*, 2013.

[2] J. Hong, M. K. Park, E. J. Lee, D. Lee, D. S. Hwang, and S. Ryu, "Origin of New Broad Raman D and G Peaks in Annealed Graphene," *Scientific Reports*, vol. 3, p. 2700, 2013.